# FOREWORD

This is the second iteration of preparing our own courseware material, after successful completion of a similar task undertaken a few years ago. These contents have been carefully prepared and should serve as excellent auxiliary material for both instructors and students.

The Special Academic Group, Autonomy (SAGA) was formed for the sole purpose of preparing courseware contents primarily in the first-year theory subjects; a few second-year subjects were also included. The subjects for the first year were - Basic Electrical Engineering, Basic Electronics Engineering, Computer Programming, Data Structures and Algorithms, Engineering Mathematics I and II, Engineering Physics, Engineering Chemistry, Constitution of India, Environmental Science and Engineering and Communicative and Technical English. For the second year, the subjects for which courseware material was prepared were Analog Electronic Circuits, Digital Systems Design, Circuit Theory and Measurements and Instruments.
Faculty members from all the departments contributed to the task. They were, in no particular order, Nalini Singh, Bimal Meher, Saumyaranjan Dash, Mukti Routray, Susmita Biswal, Manasa Dash, Bipin Tripathy, Sibasankar Nayak, Janmejay Senapati, Subrat Sahu, Pradeep Moharana, Rupambika Pattanaik, Dhananjay Tripathy, Jagadish Patra, Sachin Das, Deepak Ranjan Nayak, Amulya Roul, Bodhisattva Dash, Sanghamitra Das, Gyana Ranjan Biswal, Nibedita Swain and Rajan Mishra.

The entire group worked diligently to successfully complete the task which included a peer review of the material. I take this opportunity to thank all the members of the SAGA group for a job well done.

I sincerely hope that this courseware material comes in handy and is utilized to the fullest extent. These are readily available additional resources prepared in accordance with the Silicon autonomy syllabus, to complement textbooks and classroom lectures. If there are any errors, I would be grateful if they are brought to my notice so that we can correct them in subsequent versions.

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***December 2020***

# MODULE – 1

## Introduction to Electronics:

**Signals:** Signal is physical quantity which is a function of one or more than one independent variable like time or spatial variable. Signals convey information and include physical quantities such as voltage, current, and intensity.

Example 1: Fig.1 is a simple electrical circuit consisting of three passive components: a capacitor C, an inductor L, and a resistor R. A voltage v(t ) is applied at the input of the RLC circuit, which produces an output voltage y(t ) across the capacitor. A possible waveform for y(t ) is the sinusoidal signal. The notations v(t ) and y(t ) includes both the dependent vari able, v and y, respectively, in the two expressions, and the independent variable t . The notation v(t ) implies that the voltage v is a function of time t .

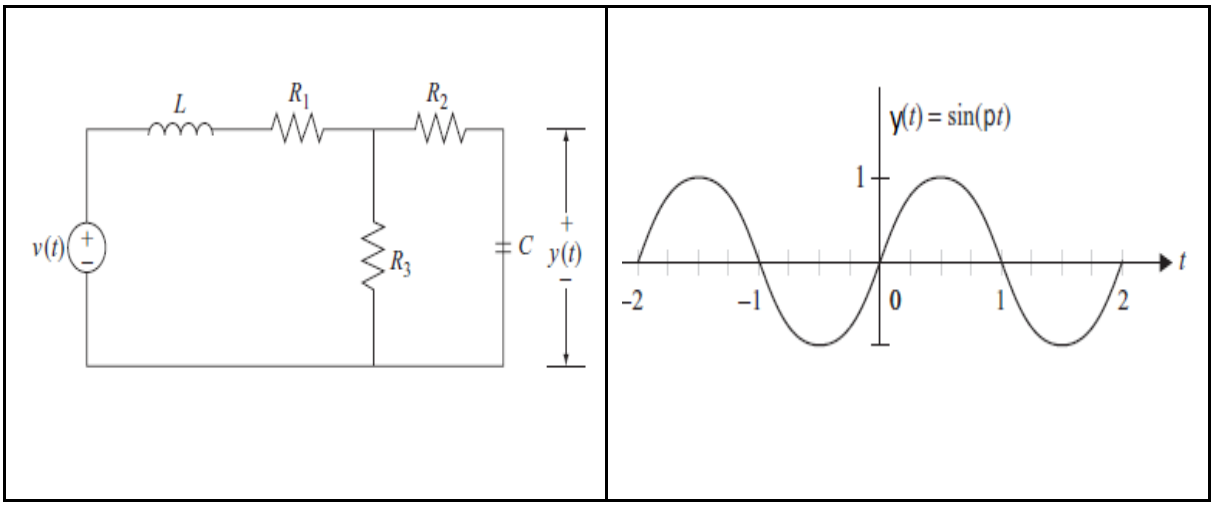



Fig.1

Example2: Fig.2 shows an audio recording system where the input signal is an audio or a speech waveform. The function of the audio recording system is to convert the audio signal into an electrical waveform, which is recorded on a magnetic tape or a compact disc. A possible resulting waveform for the recorded electrical signal is shown in right side figure of Fig 2.

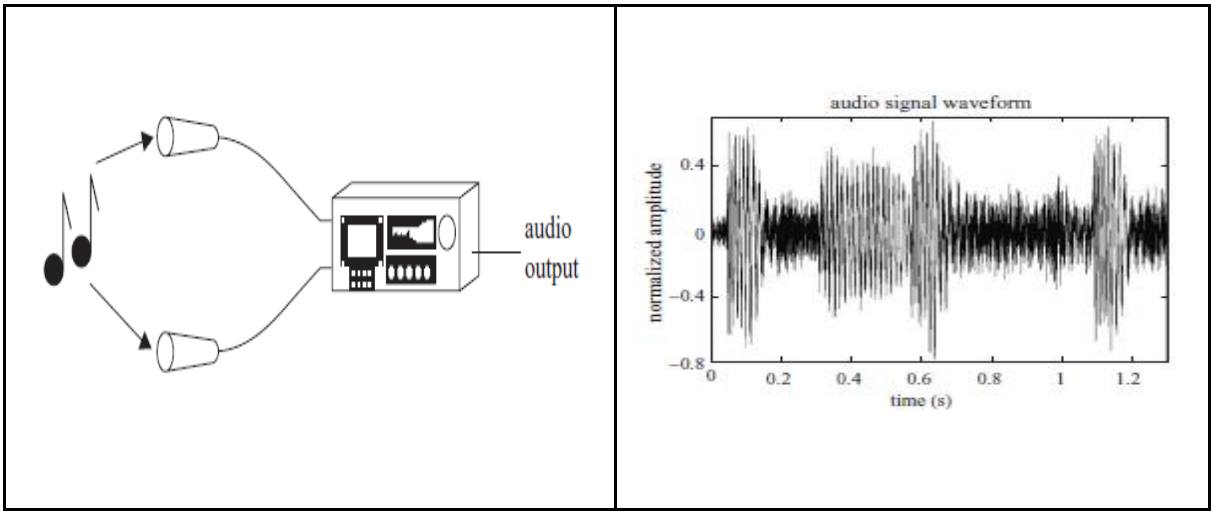



Fig.2

Example3: Fig. 3 illustrates a thermometer that measures the ambient temperature of its environment. Electronic thermometers typically use a thermal resistor, known as a thermistor, whose resistance varies with temperature. The fluctuations in the resistance are used to measure the temperature which is shown in right figure of Fig.3.

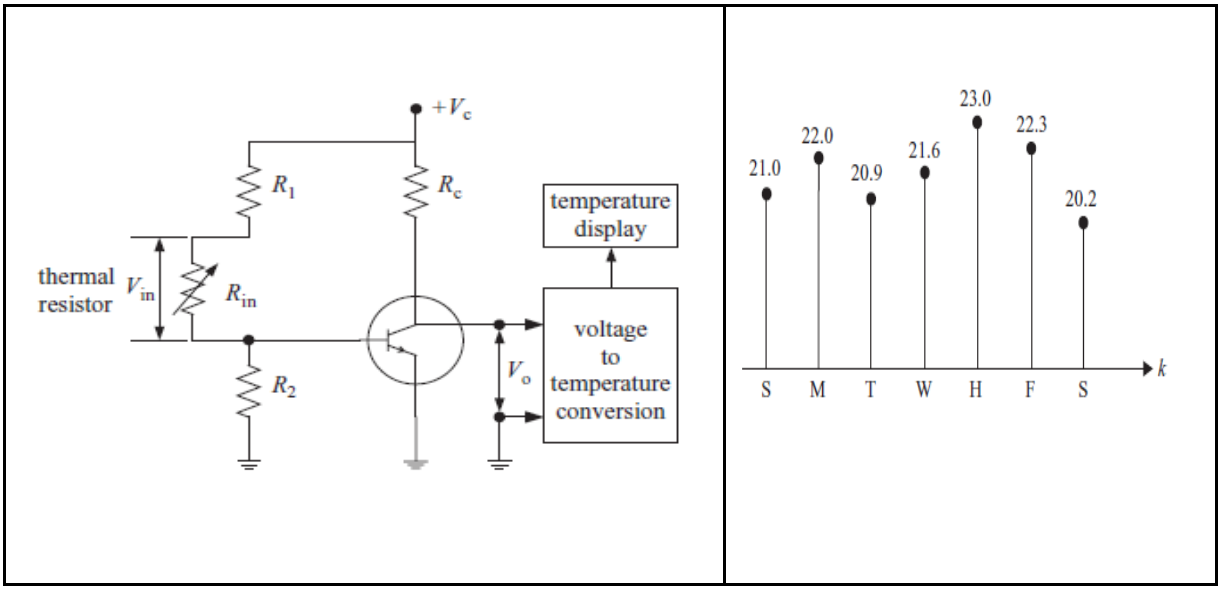



Fig.3

**Basic difference between Electrical and Electronics**

| **Electrical** | **Electronics** |
|---|---|
| • Electrical signals are having larger power or larger voltage level (220v peak to peak voltage sinusoidal signal).<br>• Electrical signals are having less frequency(50 Hz or 60 Hz)<br>• Electrical devices are very larger in size | • Electronics signals are having less power or less voltage level (mv range voltage sinusoidal signal).<br>• Electronics signals are having Larger frequency(MHz range or GHz range)<br>• Electronics devices are very smaller in size |

**Analog and Digital Signal**

**Analog Signal:** A signal is said to be Analog signal if the signal is having an infinite number of amplitude levels. The amplitudes of many real-world signals, such as voltage, current, temperature, and pressure, change continuously, and these signals are analog signals. For example, the ambient temperature of a house is an analog number that requires an infinite number of digits (e.g., 24.763 578. . . ) to record the readings precisely. The fig. 4 shown below represents an arbitrary Continuous-time analog voltage signal.

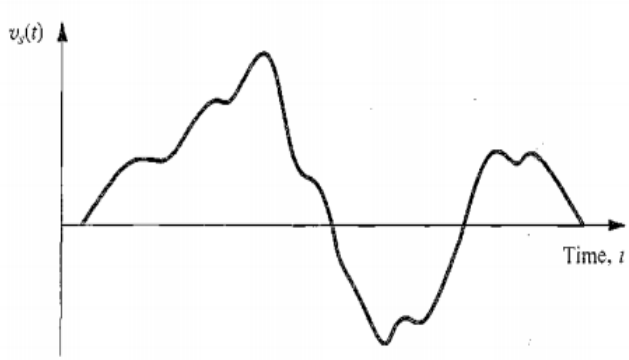



Fig.4 (An arbitrary Continuous-time analog voltage signal)

**Digital Signal:** A signal is said to be digital signal if the signal is having a finite number of amplitude levels. A digital signal is represented as a sequence of finite numbers, each number representing the signal magnitude at an instant of time. The fig. 5 shown below represents an arbitrary Continuous-time digital voltage signal.

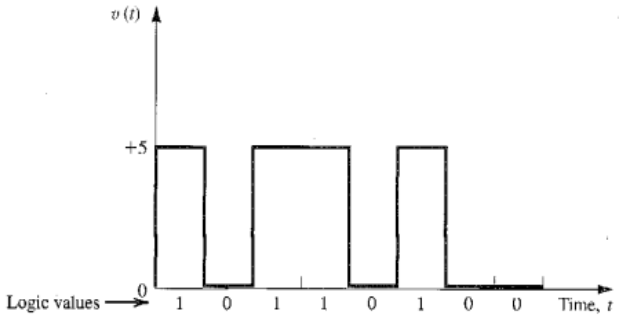



Fig.5 (Variation of a particular binary digital signal with time)

**Periodic and Non-periodic Signal**

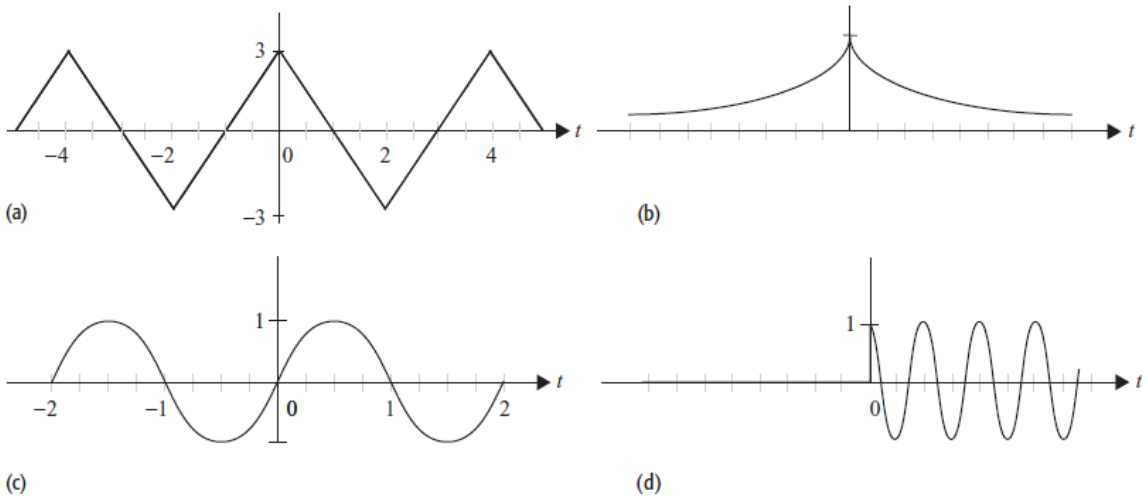
A Continuous time signal x(t) is said to be periodic if it satisfies the following properties,

1. X(t) must be an everlasting signal (i.e it exists from t=-∞ to t=∞)
2. $x(t) = x(t + nT0)$, at all time $t$ and for some positive constant $T0$ and n is an integer.

Otherwise the signal is called as Non-periodic signal.

**Note**: For any periodic signal x(t) , The smallest positive value of $T_0$ that satisfies the periodicity condition $x(t) = x(t + T_0)$, is referred to as the fundamental period of x(t).

The following figures (a) and (c) represent the periodic and figure (b) and (d) represent the Non-periodic signals.




A familiar example of a periodic signal is a sinusoidal function represented mathematically by the following expression:

$x(t) = A \sin(\omega_0 t + \theta)$,

Where A= Amplitude of x(t), $\omega_0$= Angular frequency of x(t), θ = Phase of x(t).

**Introduction to Electronics: Signals**

Example 1: Determine the peak amplitude, frequency and angular frequency of the following signals.

(a) $5 \sin 200\pi t \ volt$

(b) $-2 \cos\left(500\pi t + \frac{\pi}{4}\right) volt$

Solution:

(a) Peak amplitude of $5 \sin 200\pi t \ volt$ =5 volt

Frequency=100 Hz

Angular Frequency= $200\pi$ rad

(b) Peak amplitude of $-2 \cos\left(500\pi t + \frac{\pi}{4}\right) volt$ = 2volt

Frequency=250 Hz

Angular Frequency= $500\pi$ rad

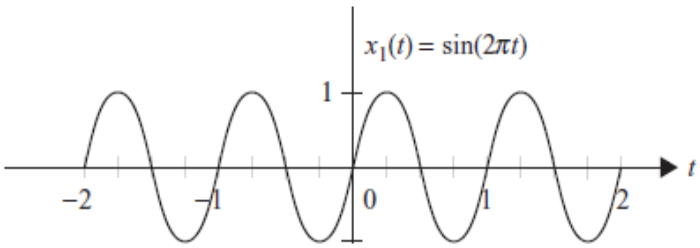
Example 2: Sketch the following signals.

(a) $x_1(t) = \sin 2\pi t \ volt$

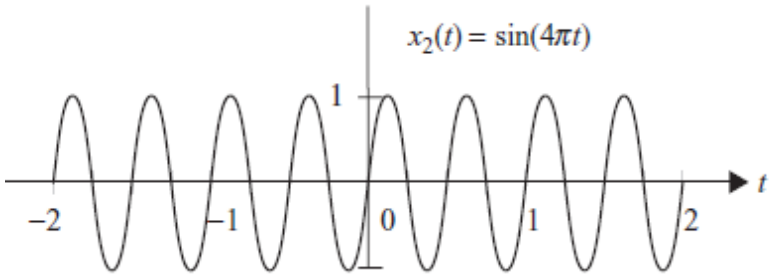
(b) $x_2(t) = \sin 4\pi t \ volt$

Solution:

(a)

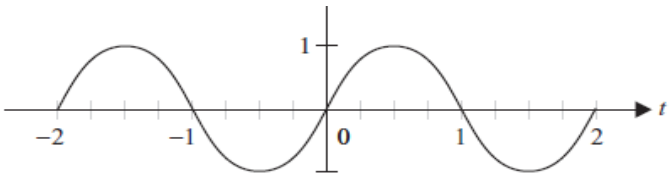



(b)

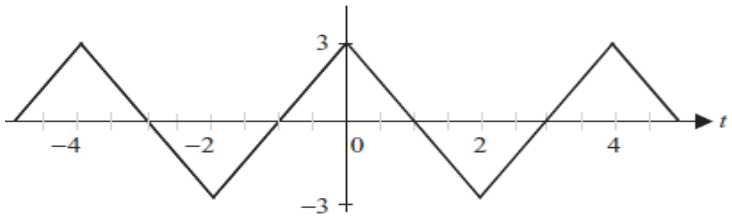



Example 3: Determine the fundamental period, fundamental frequency and peak value of the following periodic signals. [Considering amplitude in volt and 't' in sec]

(a)




(b)




Solution:

(a) Fundamental period $T_0 = 2sec$

Fundamental frequency $f_0 = \frac{1}{2}Hz$

Peak amplitude = 1 volt

(b) Fundamental period $T_0 = 4sec$

Fundamental frequency $f_0 = \frac{1}{4}Hz$

Peak amplitude = 4 volt

**Average and RMS Value Calculation:**

The average value any periodic signal $x(t)$ with period $T_0$ is defined as

$$x_{avg} = \frac{1}{T_0}\int_0^{T_0} x(t)\,dt$$

The rms (root mean square) value any periodic signal $x(t)$ with period $T_0$ is defined as

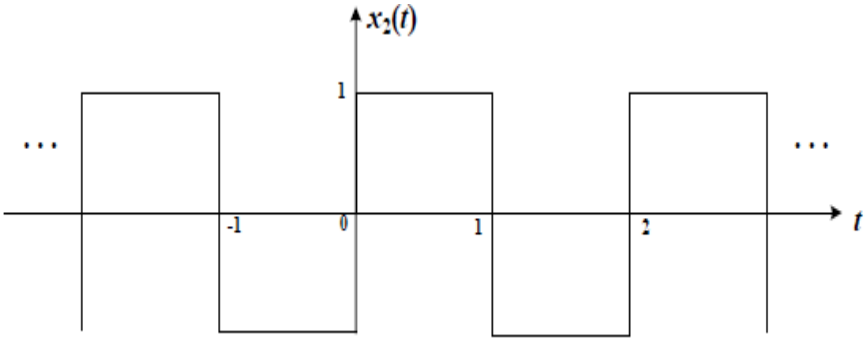
$$x_{rms} = \sqrt{\frac{1}{T_0}\int_0^{T_0} x^2(t)\,dt}$$

Example:4 Determine the average and rms value of following signals.

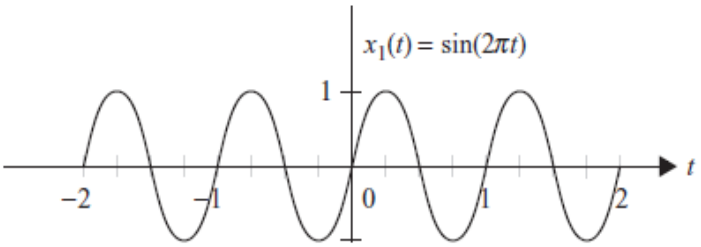
(a) X(t) = $A_m$sint

(b) X(t) = $A_m$cost

(c)




(d)




## Semiconductor

**Semiconductor**, any of a class of crystalline solids intermediate in electrical conductivity between a conductor and an insulator. Semiconductors are employed in the manufacture of various kinds of electronic devices, including diodes, transistors, and integrated circuits. Such devices have found wide application because of their compactness, reliability, power efficiency, and low cost. As discrete components, they have found use in power devices, optical sensors, and light emitters, including solid-state lasers. They have a wide range of current- and voltage-handling capabilities and, more important, lend

themselves to integration into complex but readily manufacturable microelectronic circuits. They are, and will be in the foreseeable future, the key elements for the majority of electronic systems, serving communications, signal processing, computing, and control applications in both the consumer and industrial markets.

Semiconductors do not fall into either the conductor or non-conductor categories. Instead they fall in between. A variety of materials fall into this category, and they include silicon, germanium, gallium arsenide, and a variety of other substances.

In its pure state silicon is an insulator with no free electrons in the crystal lattice. However, to understand how it acts as a semiconductor first look at the atomic structure of silicon in its pure state. Each molecule in the crystal lattice consists of a nucleus with three rings or orbits containing electrons, and each electron has a negative charge. The nucleus consists of neutrons that are neutral and have no charge, and protons that have a positive charge. In the atom there are the same number of protons and electrons so the whole atom has no overall charge.

The electrons in the silicon, as in any other element are arranged in rings with strict numbers of electrons in each orbit. The first ring can only contain two, and the second has eight. The third and outer ring of the silicon has four. The electrons in the outer shell are shared with those from adjacent atoms to make up a crystal lattice. When this happens there are no free electrons in the lattice, making silicon a good insulator. A similar picture can be seen for germanium. It has two electrons in the inner most orbit, eight in the next, 18 in the third, and four in the outer one. Again, it shares its electrons with those from adjacent atoms to make a crystal lattice without any free electrons.

**Impurities**

In order to make silicon or any other semiconductor into a partially conducting material it is necessary to add a very small amount of impurity into the material. This considerably changes the properties.

If traces of impurities of materials having five electrons in the outer ring of their atoms are added they enter the crystal lattice sharing electrons with the silicon. However as they have one extra electron in the outer ring, one electron becomes free to move around the lattice. This enables a current to flow if a potential is applied across the material. As this type of material has a surplus of electrons in the lattice it is known as an N-type semiconductor. Typical impurities that are often used to create N-type semiconductors are phosphorous and arsenic.

It is also possible to place elements with only three electrons in their outer shell into the crystal lattice. When this happens the silicon wants to share its four electrons with another atom with four atoms. However as the impurity only has three, there is a space or a hole for another electron. As this type of material has electrons missing it is known as P-type material. Typical impurities used for P-type material are boron, and aluminium.

**Holes**

It is easy to see how electrons can move around the lattice and carry a current. However it is not quite so obvious for holes. This happens when an electron from a complete orbit moves to fill a hole, leaving a hole where it came from. Another electron from another orbit can then move in to fill the new hole and so forth. The movement of the holes in one direction corresponds to a movement of electrons in the other, hence an electric current.

From this it can be seen that either electrons or holes can carry charge or an electric current. As a result, they are known as charge carriers, holes being the charge carriers for a P-type semiconductor and electrons for an N-type semiconductor.

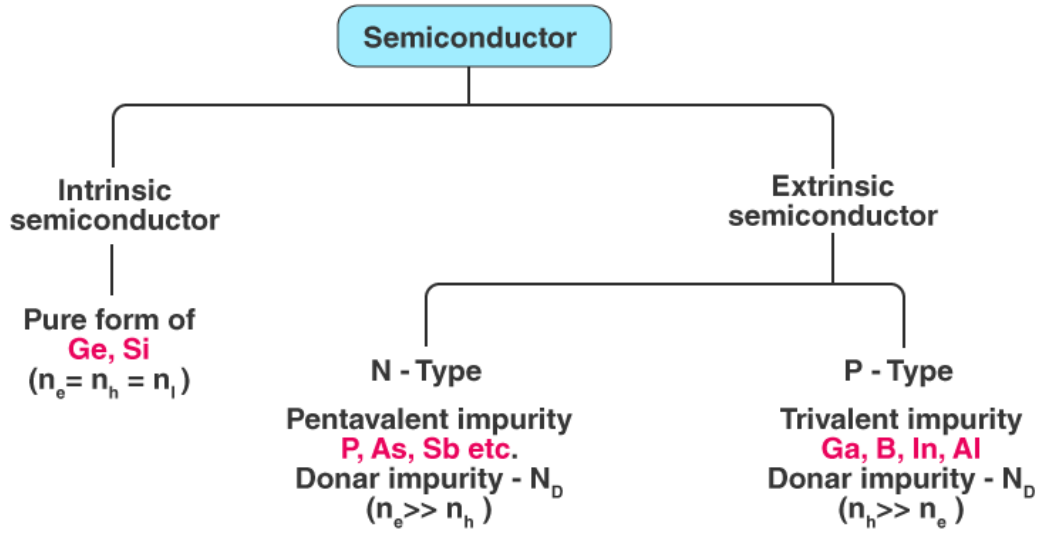
**List of common semiconductor terms**

- ***Charge carrier*** - Charge carrier is a free a free (mobile, unbound) particle carrying an electric charge, e.g. an electron or a hole.
- ***Conductor*** - A material in which electrons can move freely and electricity can flow.
- ***Electron*** - A sub-atomic particle carrying a negative charge.
- ***Hole*** - The absence of a valence electron in a semiconductor crystal. The motion of a hole is equivalent to motion of a positive charge, i.e. opposite to the motion of an electron.
- ***Insulator*** - A material in which there are no free electrons available to carry electricity.
- ***Majority carrier*** - Current carriers, either free electrons or holes that are in excess i.e. in the majority in a specific area of a semiconductor material. Electrons are the majority carriers in N-type semiconductor, and holes in a P-type area.
- ***Minority carrier*** - Current carriers, either free electrons or holes that are in the minority in a specific area of a semiconductor material
- ***N-type*** - An area of a semiconductor in which there is an excess of electrons.
- ***P-type*** - An area of a semiconductor in which there is an excess of holes.
- ***Semiconductor*** - A material that is neither an insulator nor a full conductor that has an intermediate level of electrical conductivity and in which conduction takes place by means of holes and electrons.

**Semiconductors types / classifications**

There are two basic groups or classifications that can be used to define the different semiconductor types:

***Intrinsic material:*** An intrinsic type of semiconductor material made to be very pure chemically. As a result, it possesses a very low conductivity level having very few numbers of charge carriers, namely holes and electrons, which it possesses in equal quantities.




**Classification of Semiconductors**

**Atomic structure of silicon and germanium**

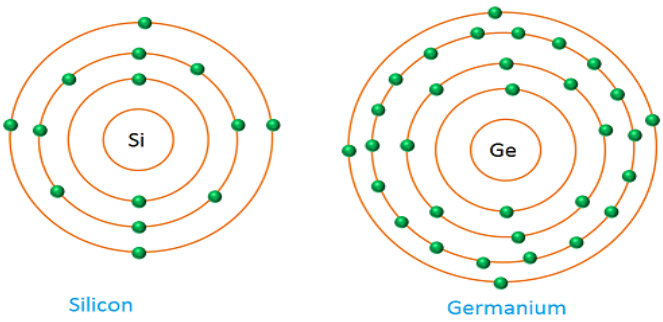
The atomic structure of intrinsic semiconductor materials like silicon and germanium is as follows.

**Atomic structure of silicon**

Silicon is a substance consisting of atoms which all have the same number of protons. The atomic number of silicon is 14 i.e. 14 protons. The number of protons in the nucleus of an atom is called atomic number. Silicon atom has 14 electrons (two electrons in first orbit, eight electrons in second orbit and 4 electrons in the outermost orbit).

**Atomic structure of germanium**

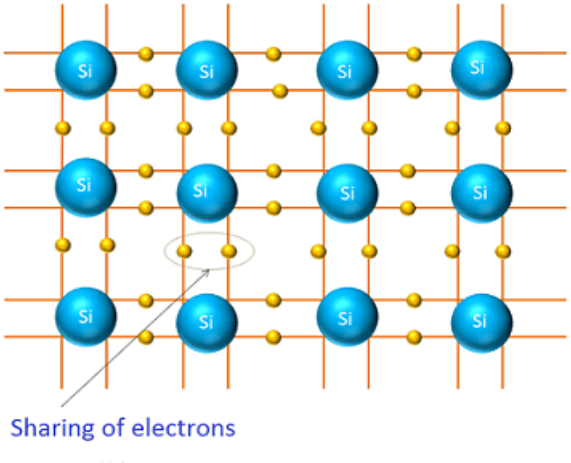
Germanium is a substance consisting of atoms which all have the same number of protons. The atomic number of germanium is 32 i.e. 32 protons. The number of protons in the nucleus of atom is called atomic number. Germanium has 32 electrons (2 electrons in first orbit, 8 electrons in second orbit, 18 electrons in third orbit and 4 electrons in the outermost orbit.




## Covalent bonding in silicon and germanium

### Covalent bonding in silicon

The outermost shell of atom is capable to hold up to eight electrons. The atom which has eight electrons in the outermost orbit is said to be completely filled and most stable. But the outermost orbit of silicon has only four electrons. Silicon atom needs four more electrons to become most stable. Silicon atom forms four covalent bonds with the four neighbouring atoms. In covalent bonding each valence electron is shared by two atoms.



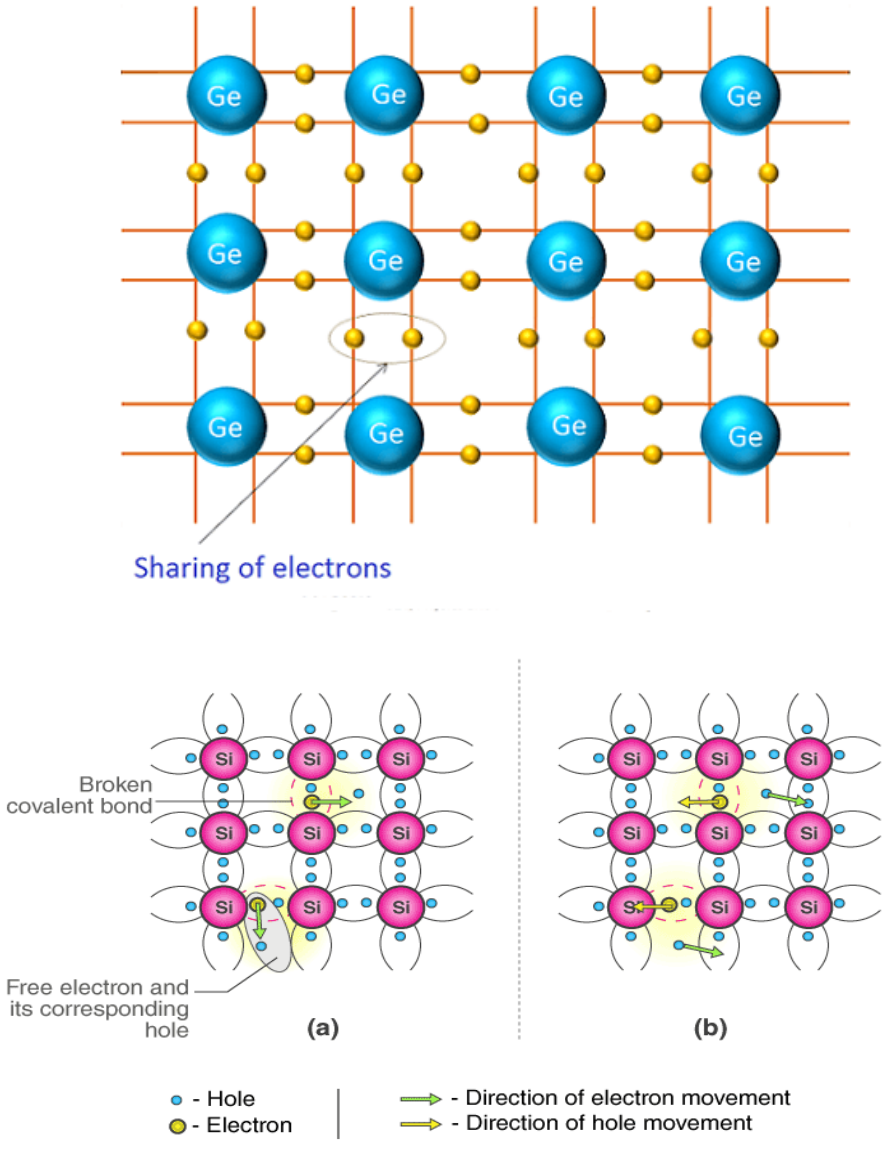

When silicon atoms comes close to each other, each valence electron of atom is shared with the neighbouring atom and each valence electron of neighbouring atom is shared with this atom. Likewise each atom will share four valence electrons with the four neighbouring atoms and four neighbouring atoms will share each valence electron with this atom. Therefore, total eight electrons are shared.

### Covalent bonding in germanium

The outermost orbit of germanium has only four electrons. Germanium atom needs four more electrons to become most stable. Germanium atom forms four covalent bonds with the four neighbouring atoms. In covalent bonding each valence electron is shared by two atoms.

When germanium atoms comes close to each other each valence electron of atom is shared with the neighbouring atom and each valence electron of neighbouring atom is shared with this atom. Likewise each atom will share four valence electrons with the four neighbouring atoms and four neighbouring atoms will share each valence electron with this atom. Therefore, total eight electrons are shared.

The outermost shell of silicon and germanium is completely filled and valence electrons are tightly bound to the nucleus of atom because of sharing electrons with neighboring atoms. In intrinsic semiconductors free electrons are not present at absolute zero temperature. Therefore intrinsic semiconductor behaves as perfect insulator.




**Conduction Mechanism in Case of Intrinsic Semiconductors (a) In absence of electric field (b) In presence of electric Field**

***Extrinsic material:*** Extrinsic types of semiconductor are those where a small amount of impurity has been added to the basic intrinsic material. This 'doping' uses an element from a different periodic table group and in this way it will either have more or less electrons in the valence band than the semiconductor itself. This creates either an excess or shortage of electrons. In this way two types of semiconductor are available: Electrons are negatively charged carriers.

**Types of impurities**

Two types of impurities are added to the semiconductor. They are pentavalent and trivalent impurities.

1. **Pentavalent impurities**

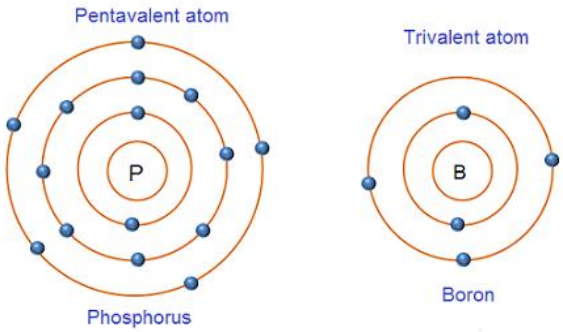
   Pentavalent impurity atoms have 5 valence electrons. The various examples of pentavalent impurity atoms include Phosphorus (P), Arsenic (As), Antimony (Sb), etc. The atomic structure of pentavalent atom (phosphorus) and trivalent atom (boron) is shown in below fig.

Phosphorus is a substance consisting of atoms which all have the same number of protons. The atomic number of phosphorus is 15 i.e. 15 protons. The number of protons in the nucleus of an atom is called atomic number. Phosphorus atom has 15 electrons (2 electrons in first orbit, 8 electrons in second orbit and 5 electrons in the outermost orbit).

2. **Trivalent impurities**

   Trivalent impurity atoms have 3 valence electrons. The various examples of trivalent impurities include Boron (B), Gallium (G), Indium(In), Aluminium (Al).

Boron is a substance consisting of atoms which all have the same number of protons. The atomic number of boron is 5 i.e. 5 protons. Boron atom has 5 electrons (2 electrons in first orbit and 3 electrons in the outermost orbit).



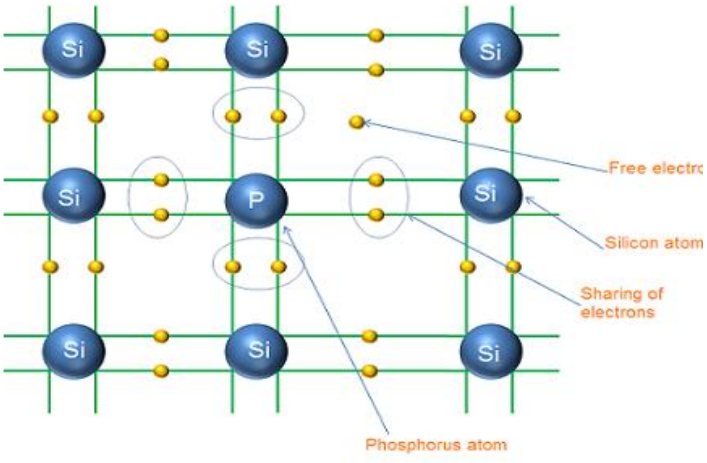

***N-type:***

An N-type semiconductor material has an excess of electrons. In this way, free electrons are available within the lattices and their overall movement in one direction under the influence

of a potential difference results in an electric current flow. This in an N-type semiconductor, the charge carriers are electrons.

When pentavalent impurity is added to an intrinsic or pure semiconductor (silicon or germanium), then it is said to be an n-type semiconductor. Pentavalent impurities such as phosphorus, arsenic, antimony etc are called donor impurity.

Let us consider, pentavalent impurity phosphorus is added to silicon as shown in below figure. Phosphorus atom has 5 valence electrons and silicon has 4 valence electrons. Phosphorus atom has one excess valence electron than silicon. The four valence electrons of each phosphorus atom form 4 covalent bonds with the 4 neighboring silicon atoms. The fifth valence electron of the phosphorus atom cannot able to form the covalent bond with the silicon atom because silicon atom does not have the fifth valence electron to form the covalent bond. Thus, fifth valence electron of phosphorus atom does not involve in the formation of covalent bonds. Hence, it is free to move and not attached to the parent atom.



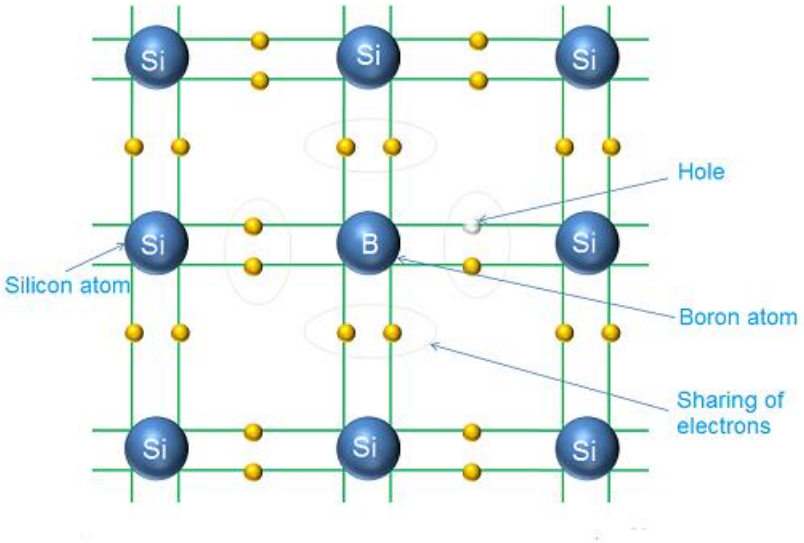

This shows that each phosphorus atom donates one free electron. Therefore, all the pentavalent impurities are called donors. The number of free electrons are depends on the amount of impurity (phosphorus) added to the silicon. A small addition of impurity (phosphorus) generates millions of free electrons.

***P-type:***

In a P-type semiconductor material there is a shortage of electrons, i.e. there are 'holes' in the crystal lattice. Electrons may move from one empty position to another and in this case it can be considered that the holes are moving. This can happen under the influence of a potential difference and the holes can be seen to flow in one direction resulting in an electric current flow. It is actually harder for holes to move than for free electrons to move and therefore the mobility of holes is less than that of free electrons. Holes are positively charged carriers.

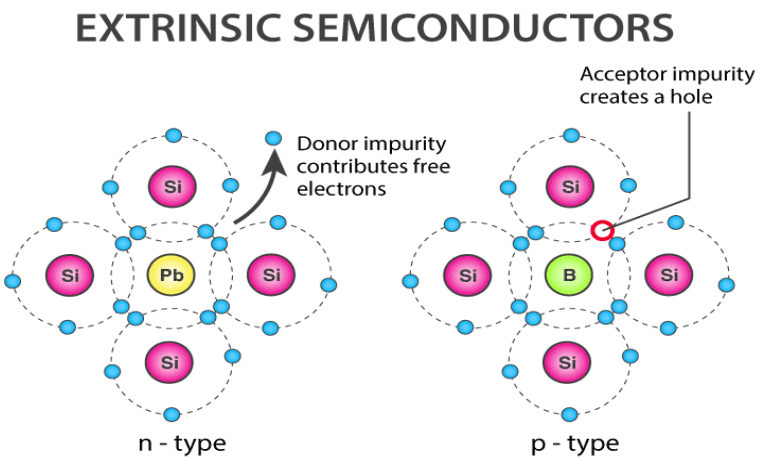
When the trivalent impurity is added to an intrinsic or pure semiconductor (silicon or germanium), then it is said to be p-type semiconductor. Trivalent impurities such as Boron (B), Gallium (G), Indium(In), Aluminium(Al) etc are called acceptor impurity.

Let us consider, trivalent impurity boron is added to silicon as shown in below figure. Boron atom has three valence electrons and silicon has four valence electrons. The three valence electrons of each boron atom form 3 covalent bonds with the 3 neighbouring silicon atoms.




In the fourth covalent bond, only silicon atom contributes one valence electron, while the boron atom has no valence electron to contribute. Thus, the fourth covalent bond is incomplete with shortage of one electron. This missing electron is called hole.

This shows each boron atom accept one electron to fill the hole. Therefore, all the trivalent impurities are called acceptors. A small addition of impurity (boron) provides millions of holes.




**Classification of Extrinsic Semiconductor**

**Semiconductor material groups**

Most commonly used semiconductor materials are crystalline inorganic solids. These materials are often classified according to their position or group within the periodic table. These groups are determined by the electrons in the outer orbit the particular elements.

While most semiconductor materials used are inorganic, a growing number of organic materials are also being investigated and used.

**Semiconductor materials list**

There are many different types of semiconductor materials that can be used within electronic devices. Each has its own advantages, disadvantages and areas where it can be used to offer the optimum performance.

| Material | Chemical Symbol / formula | Group | Details |
|---|---|---|---|
| Germanium | Ge | IV | This type of semiconductor material was used in many early devices from radar detection diodes to the first transistors. Diodes show a higher reverse conductivity and temperature coefficient meant that early transistors could suffer from thermal runaway. Offers a better charge carrier mobility than silicon and is therefore used for some RF devices. Not as widely used these days as better semiconductor materials are available. |
| Silicon | S | IV | Silicon is the most widely used type of semiconductor material. Its major advantage is that it is easy to fabricate and provides good general electrical and mechanical properties. Another advantage is that when it is used for integrated circuits it forms high quality silicon oxide that is used for insulation layers between different active elements of the IC. |
| Gallium arsenide | GaAs | III-V | Gallium arsenide is the second most widely used type of semiconductor after silicon. It is widely used in high performance RF devices where its high electron mobility is utilised. It is also used as substrate for other III-V semiconductors, e.g. InGaAs and GaInNAs. However it is a brittle material and has a lower hole mobility than Silicon which makes applications such as P-type CMOS transistors not feasible. It is also relatively difficult to fabricate and this increases the costs of GaAs devices. |
| Silicon carbide | SiC | IV | Silicon carbide finds uses in a number of applications. It is often used in power devices where its losses are significantly lower and operating temperatures can be higher than those of silicon based devices. Silicon carbide has a breakdown |

| Material | Chemical Symbol / formula | Group | Details |
|---|---|---|---|
| | | | capability which is about ten times that of silicon itself. Forms of silicon carbide were types of semiconductor material that were used with some early forms of yellow and blue LEDs. |
| Gallium Nitride | GaN | III-V | This type of semiconductor material is starting to be more widely in microwave transistors where high temperatures and powers are needed. It is also being used in some microwave ICs. GaN is difficult to dope to give p-type regions and it is also sensitive to ESD, but relatively insensitive to ionising radiation. Has been used in some blue LEDs. |
| Gallium phosphide | GaP | III-V | This semiconductor material has found many uses within LED technology. It was used in many early low to medium brightness LEDs producing a variety of colours dependent upon the addition of other dopants. Pure Gallium phosphide produces a green light, nitrogen-doped, it emits yellow-green, ZnO-doped it emits red. |
| Cadmium sulphide | CdS | II-VI | Used in photo resistors and also solar cells. |
| Lead sulphide | PbS | IV-VI | Used as the mineral galena, this semiconductor material was used in the very early radio detectors known as 'Cat's Whiskers' where a point contact was made with the tin wire onto the galena to provide rectification of the signals. |

It is easy to see how electrons can move around the lattice and carry a current. However it is not quite so obvious for holes. This happens when an electron from a complete orbit moves to fill a hole, leaving a hole where it came from. Another electron from another orbit can then move in to fill the new hole and so forth. The movement of the holes in one direction corresponds to a movement of electrons in the other, hence an electric current.

From this it can be seen that either electrons or holes can carry charge or an electric current. As a result, they are known as charge carriers, holes being the charge carriers for a P-type semiconductor and electrons for an N-type semiconductor.

**Examples of Semiconductors:**

**Gallium arsenide**, **germanium**, and **silicon** are some of the most **commonly used semiconductors**. Silicon is used in electronic circuit fabrication and gallium arsenide is used in solar cells, laser diodes, etc.

**Holes and Electrons in Semiconductors**

**Holes and electrons** are the types of charge carriers accountable for the flow of current in semiconductors. **Holes** (valence electrons) are the positively charged electric charge carrier

whereas **electrons** are the negatively charged particles. Both electrons and holes are equal in magnitude but opposite in polarity.

**Mobility of Electrons and Holes**

In a semiconductor, the **mobility of electrons is higher than that of the holes**. It is mainly because of their different band structures and scattering mechanisms.

Electrons travel in the conduction band whereas holes travel in the valence band. When an electric field is applied, holes cannot move as freely as electrons due to their restricted movement. The elevation of electrons from their inner shells to higher shells results in the creation of holes in semiconductors. Since the holes experience stronger atomic force by the nucleus than electrons, holes have lower mobility.

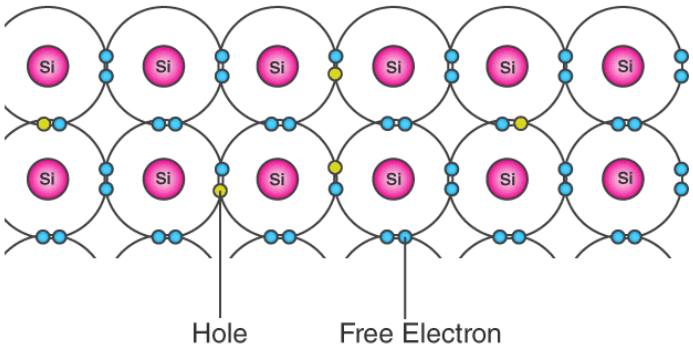
The mobility of a particle in a semiconductor is more if;

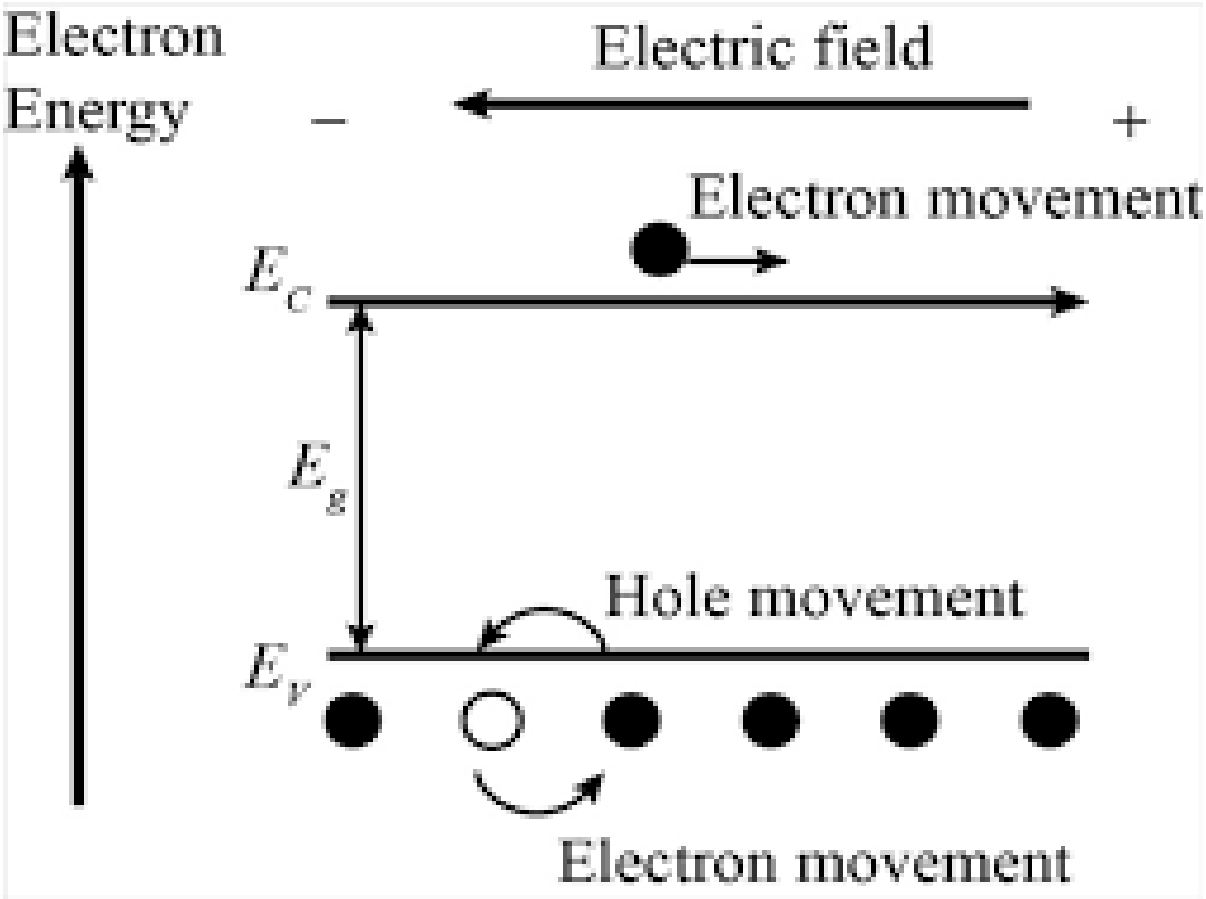
- Effective mass of particles is lesser
- Time between scattering events is more

For intrinsic silicon at 300 K, the mobility of electrons is 1500 $cm^2 (V \cdot s)^{-1}$ and the mobility of holes is 475 $cm^2 (V \cdot s)^{-1}$.

The **bond model** of electrons in silicon of valency 4 is shown below. Here, when one of the free electrons (blue dots) leaves the lattice position, it creates a hole (grey dots). This hole thus created takes the opposite charge of the electron and can be imagined as positive charge carriers moving in the lattice.

**Concept of Electrons and Holes in Semiconductors**

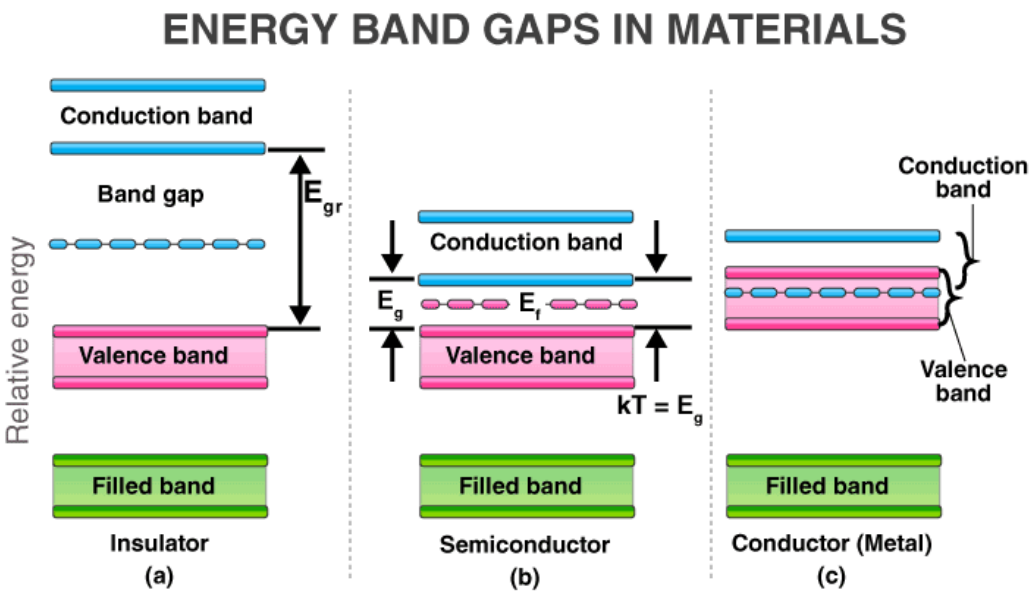





**Band Theory of Semiconductors**

The introduction of band theory happened during the quantum revolution in science. Walter Heitler and Fritz London discovered the energy bands.

We know that the electrons in an atom are present in different energy level. When we try to assemble a lattice of a solid with N atoms, then each level of an atom must split up into N levels in the solid. This splitting up of sharp and tightly packed energy levels forms **Energy Bands**. The gap between adjacent bands representing a range of energies that possess no electron is called a **Band Gap**.




## Conduction Band and Valence Band in Semiconductors

***Valence Band**:*

The energy band involving the energy levels of valence electrons is known as the valence band. It is the highest occupied energy band. When compared with insulators, the bandgap in semiconductors is smaller. It allows the electrons in the valence band to jump into the conduction band on receiving any external energy.

***Conduction Band:***

It is the lowest unoccupied band that includes the energy levels of positive (holes) or negative (free electrons) charge carriers. It has conducting electrons resulting in the flow of current. The conduction band possess high energy level and are generally empty. The conduction band in semiconductors accepts the electrons from the valence band.

**What is Fermi Level in Semiconductors?**

Fermi level (denoted by EF) is present between the valence and conduction bands. It is the highest occupied molecular orbital at absolute zero. The charge carriers in this state have their own quantum states and generally do not interact with each other. When the temperature rises above absolute zero, these charge carriers will begin to occupy states above Fermi level.

In a **p-type semiconductor**, there is an increase in the density of unfilled states. Thus, accommodating more electrons at the lower energy levels. However, in an **n-type semiconductor**, the density of states increases, therefore, accommodating more electrons at higher energy levels.

**Properties of Semiconductors**

Semiconductors can conduct electricity under preferable conditions or circumstances. This unique property makes it an excellent material to conduct electricity in a controlled manner as required.

Unlike conductors, the charge carriers in semiconductors arise only because of external energy (thermal agitation). It causes a certain number of valence electrons to cross the energy gap and jump into the conduction band, leaving an equal amount of unoccupied energy states, i.e. holes. Conduction due to electrons and holes are equally important.

- **Resistivity:** $10^{-5}$ to $10^{6}$ Ωm
- **Conductivity:** $10^{5}$ to $10^{-6}$ mho/m
- **Temperature coefficient of resistance:** Negative
- **Current Flow:** Due to electrons and holes

**Why does the Resistivity of Semiconductors go down with Temperature?**

The difference in resistivity between conductors and semiconductors is due to their difference in charge carrier density.

The resistivity of semiconductors decreases with temperature because the number of charge carriers increases rapidly with increase in temperature making the fractional change i.e. the temperature coefficient negative.

**Some Important Properties of Semiconductors are:**

1. Semiconductor acts like an insulator at Zero Kelvin. On increasing the temperature, it works as a conductor.
2. Due to their exceptional electrical properties, semiconductors can be modified by doping to make semiconductor devices suitable for energy conversion, switches, and amplifiers.
3. Lesser power losses.
4. Semiconductors are smaller in size and possess less weight.
5. Their resistivity is higher than conductors but lesser than insulators.
6. The resistance of semiconductor materials decreases with the increase in temperature and vice-versa.

**Majority & minority carriers**

**What is charge carrier?**

Generally, carrier refers to any object that carry another object from one place to another place. For example, in countries such as India, Singapore and Brazil: Tiffin box or Tiffin carriers are widely used for carrying food from one place to another place. Here, the Tiffin box acts as a carrier that carries the food from one place to another place.

Let us take another example; People use vehicles such as buses, trains, airplanes, etc. to travel from one place to another place. Here, the vehicles act as carriers that carry people from one place to another place. In the similar way, particles such as free electrons and holes carry the charge or electric current from one place to another place.

**Negative charge carriers**

The negative charge carriers such as free electrons are the charge carriers that carry negative charge with them while moving from one place to another place. Free electrons are the electrons that are detached from the parent atom and moves freely from one place to another place.

**Positive charge carriers**

The positive charge carriers such as holes are the charge carriers that carry positive charge with them while moving from one place to another place. Holes are the vacancies in valence band that moves from one place to another place within the valence band.

**Majority and minority charge carriers definition**

The charge carriers that are present in large quantity are called majority charge carriers. The majority charge carriers carry most of the electric charge or electric current in the semiconductor. Hence, majority charge carriers are mainly responsible for electric current flow in the semiconductor.

The charge carriers that are present in small quantity are called minority charge carriers. The minority charge carriers carry very small amount of electric charge or electric current in the semiconductor.

**Charge carriers in intrinsic semiconductor**

The semiconductors that are in pure form are called intrinsic semiconductors. In intrinsic semiconductor the total number of negative charge carriers (free electrons) is equal to the total number of positive charge carriers (holes or vacancy).

**Total negative charge carriers = Total positive charge carriers**

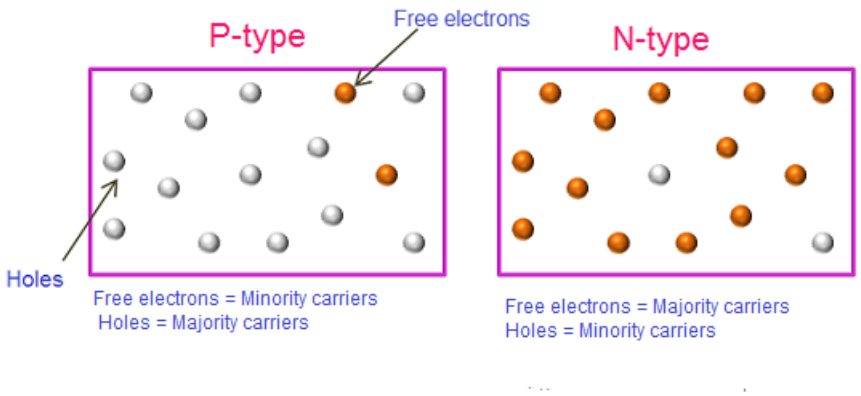
**Majority and minority charge carriers in n-type semiconductor**

When the pentavalent atoms such as Phosphorus or Arsenic are added to the intrinsic semiconductor, an n-type semiconductor is formed. In n-type semiconductor, large number of free electrons is present. Hence, free electrons are the majority charge carriers in the n-type semiconductor. The free electrons (majority charge carriers) carry most of the electric charge or electric current in the n-type semiconductor.

In n-type semiconductor, very small number of holes is present. Hence, holes are the minority charge carriers in the n-type semiconductor. The holes (minority charge carriers) carry only a small amount of electric charge or electric current in the n-type semiconductor.

The total number of negative charge carriers (free electrons) in n-type semiconductor is greater than the total number of positive charge carriers (holes) in the n-type semiconductor.

**Total negative charge carriers > Total positive charge carriers**




**Majority and minority charge carriers in p-type semiconductor**

When the trivalent atoms such as Boron or Gallium are added to the intrinsic semiconductor, a p-type semiconductor is formed. In p-type semiconductor, large number of holes is present. Hence, holes are the majority charge carriers in the p-type semiconductor. The holes (majority charge carriers) carry most of the electric charge or electric current in the p-type semiconductor.

In p-type semiconductor, very small number of free electrons is present. Hence, free electrons are the minority charge carriers in the p-type semiconductor. The free electrons (minority charge carriers) carry only a small amount of electric current in the p-type semiconductor.

The total number of negative charge carriers (free electrons) in p-type semiconductor is less than the total number of positive charge carriers (holes) in the p-type semiconductor.

**Total negative charge carriers < Total positive charge carriers**

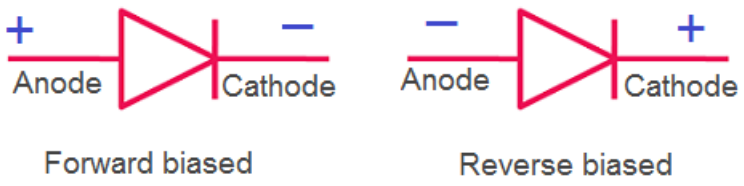
**P-N junction semiconductor diode**

A p-n junction diode is two-terminal or two-electrode semiconductor device, which allows the electric current in only one direction while blocks the electric current in opposite or reverse direction. If the diode is forward biased, it allows the electric current flow. On the other hand, if the diode is reverse biased, it blocks the electric current flow. P-N junction semiconductor diode is also called as p-n junction semiconductor device.

In n-type semiconductors, free electrons are the majority charge carriers whereas in p-type semiconductors, holes are the majority charge carriers. When the n-type semiconductor is joined with the p-type semiconductor, a p-n junction is formed. The p-n junction, which is formed when the p-type and n-type semiconductors are joined, is called as p-n junction diode.

The p-n junction diode is made from the semiconductor materials such as silicon, germanium, and gallium arsenide. For designing the diodes, silicon is more preferred over germanium. The p-n junction diodes made from silicon semiconductors works at higher temperature when compared with the p-n junction diodes made from germanium semiconductors.

The basic symbol of p-n junction diode under forward bias and reverse bias is shown in the below figure.




In the above figure, arrowhead of a diode indicates the conventional direction of electric current when the diode is forward biased (from positive terminal to the negative terminal). The holes which moves from positive terminal (anode) to the negative terminal (cathode) is the conventional direction of current.

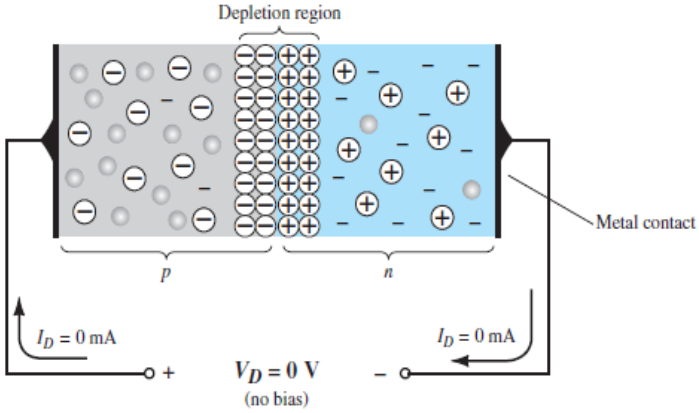
The free electrons moving from negative terminal (cathode) to the positive terminal (anode) actually carry the electric current. However, due to the convention we have to assume that the current direction is from positive terminal to the negative terminal.

## SEMICONDUCTOR DIODE

The first solid-state electronic device: The *semiconductor diode* can be constructed by simply joining an *n* -type and a *p* -type material together where one is having majority carrier of electrons and other with a majority carrier of holes. For its operation, in three different ways an external potential difference can be applied. This application of an external voltage across the two terminals of the device to extract a response is termed as *bias*.

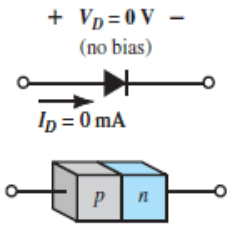
**(a) No Bias is Applied ( $V_D$ =0 V)**

At the instant the two materials are "joined" the electrons and the holes in the region of the junction will combine, resulting in a lack of free carriers in the region near the junction, as shown in Figure below.




(Fig. An internal distribution of charge with no external bias for a pn- junction)

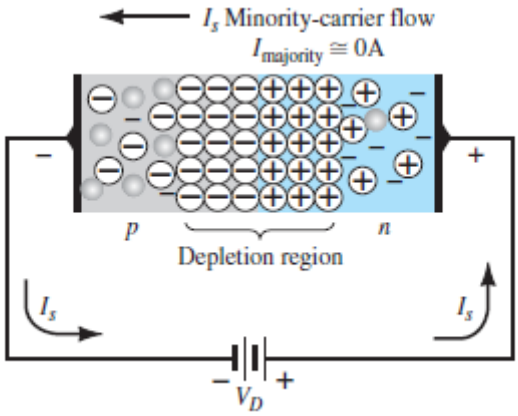
This region of uncovered positive and negative ions is called the depletion region due to the "depletion" of free carriers in the region. If leads are connected to the ends of each material, a *two-terminal device* results, as shown in Figure below. It is simply a diode with two leads sitting isolated.




(Fig. a diode symbol, with the polarity and the current direction when $V_D$ = 0 V )

**(b) Reverse-Bias Condition ( $V_D$ =0 V)**

When an external potential of $V_D$ volts is applied across the *p* – *n* junction such that the positive terminal is connected to the *n* -type material and the negative terminal is connected to the *p* -type material as shown in Figure below , then it is called as reverse bias condition.



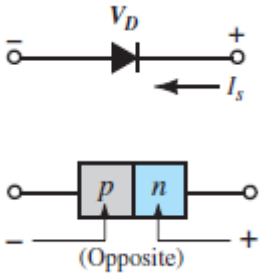

(Fig. An internal distribution of charge under reverse-bias conditions for a p–n junction)

When this negative bias voltage $V_D$ is applied, the number of uncovered positive ions in the depletion region of the *n* -type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage. Similarly due to same reasons, the number of uncovered negative ions will increase in the *p* -type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish a great barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero, as shown in Figure above.

The number of *minority carriers*, that find themselves entering the depletion region will not change, resulting in minority-carrier flow with magnitude same as no bias condition.

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by $I_s$ . $I_s$ is in nA range for Si and µA range for Ge.

The reverse-biased conditions are depicted in Figure below for the diode symbol and *pn*-junction.

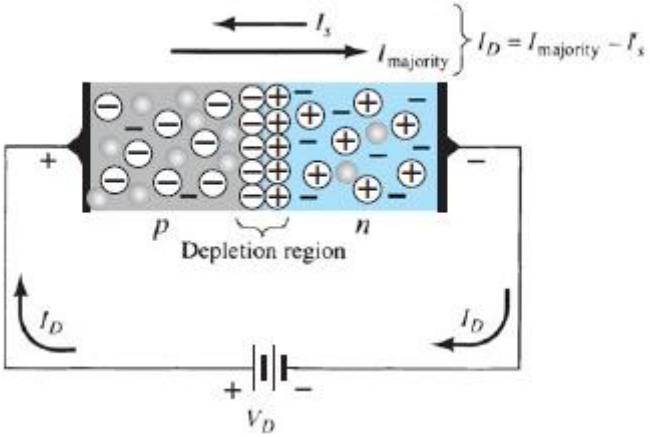



(Fig. A diode symbol, with the polarity and the current direction when $V_D < 0$ V )

As shown in Figure above, the direction of $I_s$ is against the arrow of the symbol.

**(c) Forward-Bias Condition ( $V_D > 0$ V)**

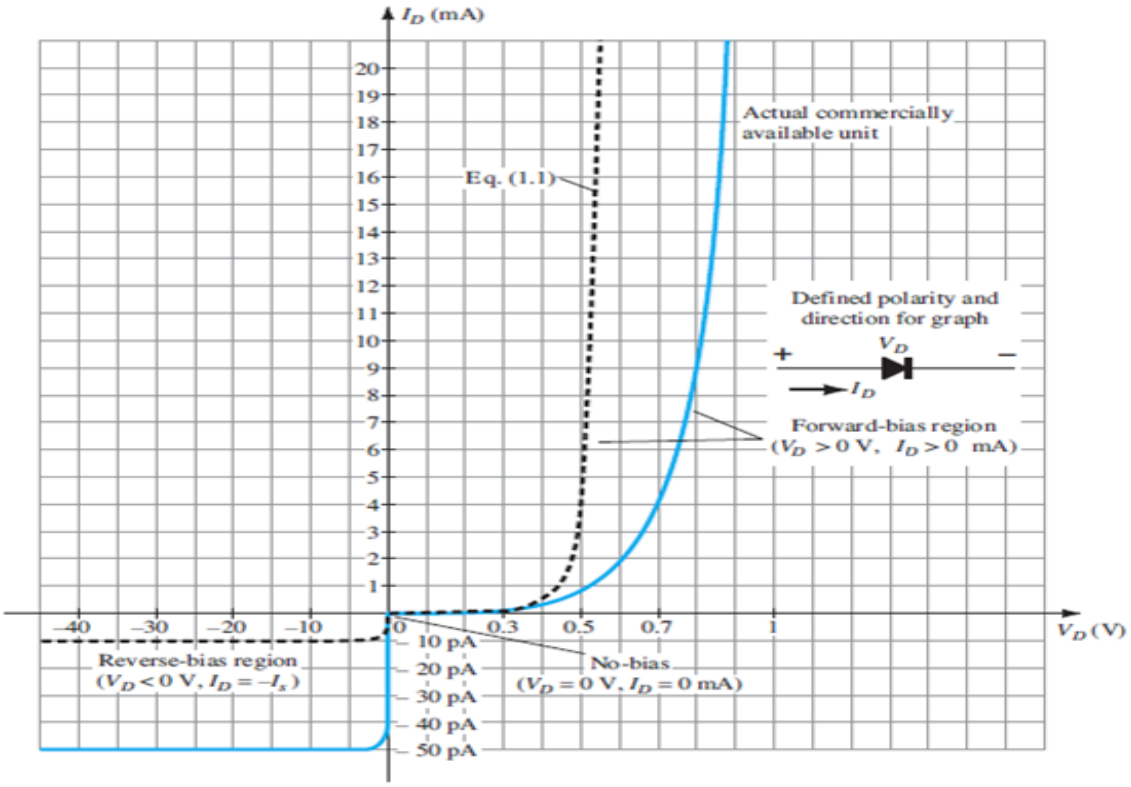
A *forward-bias* or "on" condition is established by applying the positive potential to the *p* -type material and the negative potential to the *n* -type material as shown in Figure below.




**(**Fig. An internal distribution of charge under forward-bias conditions for a p–n junction)

The application of a forward-bias potential $V_D$ will "pressure" electrons in the *n* -type material and holes in the *p* -type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Figure above. The resulting minority-carrier flow of electrons from the *p* -type material to the *n* -type material (and of holes from the *n* –type material to the *p* -type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction.

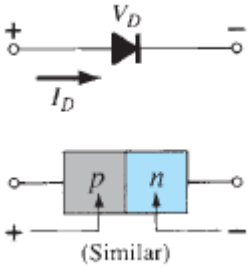
As the applied bias increases in magnitude, the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting in an exponential rise in current as shown in the forward-bias region of the characteristics of Figure below.




(Fig. Silicon semiconductor diode characteristics)

In this above Figure, vertical scale is measured in milli-amperes and the horizontal scale in the forward-bias region has a maximum of 1 V.

Typically, therefore, the voltage across a forward-biased diode will be less than 1 V.
The forward-biased conditions are depicted in Figure below for the diode symbol and *pn*-junction.




(Fig. Forward-biased p–n junction, forward-bias polarity and direction of resulting current)

This forward- and reverse-bias region of a semiconductor diode can be expressed by the equation

$$I_D = I_s\left(e^{\frac{V_D}{nV_T}} - 1\right) \text{ A} \qquad \text{----------(1)}$$

where $I_s$ is the reverse saturation current

$V_D$ is the applied forward-bias voltage across the diode

n is an ideality factor and is a function of the operating conditions and physical construction; it has a range between 1 and 2 depending on a wide variety of factors.

The voltage $V_T$ in Eq. (1) is called the *thermal voltage* and is determined by

$$V_T = \frac{kT_k}{q} \text{ V} \qquad \text{----------(2)}$$

where *k* is Boltzmann's constant = 1.38 x $10^{-23}$ J/K

$T_K$ is the absolute temperature in kelvins =273+the temperature in °C

*q* is the magnitude of electronic charge = 1.6 x $10^{-19}$ C

The plot of Eq.1 is as shown in Fig.6. From this Eq.1, if $V_D$ is positive, then $I_D$ is positive and curve will rise as the function $y = e^x$.

If $V_D = 0$V, then $I_D$=0mA as shown in Figure above.

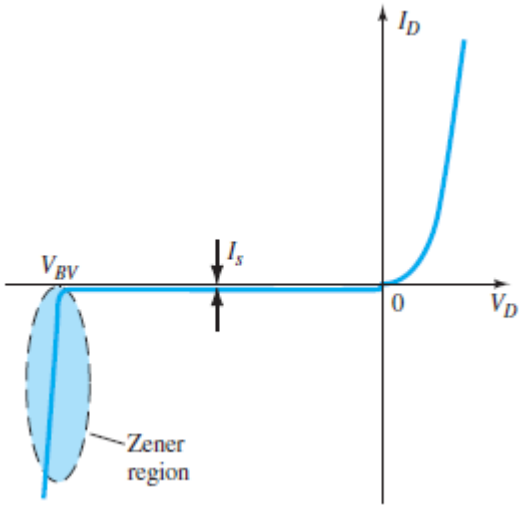
If $V_D$= -ve voltage, then 1st term will quickly drop off below $I_s$, then $I_D = -I_S$ which is a horizontal line.

**[Note:- Knee voltage- the forward voltage at which the current through the junction starts to increase rapidly. It is 0.7v for Si, 0.3v for Ge diode and 1.2 v for GaAs**

**Reverse voltage- the minimum reverse voltage at which the pn-junction brakes down with sudden rise in reverse current]**

**Breakdown Region:**

The diode characteristic figure is having a negative region. In the negative region, there is a point where the application of too negative a voltage results in a sharp change in the characteristics, as shown in Figure below.




(Fig. Breakdown region)

The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the *breakdown potential* or *Zener Potential* and is given the symbol $V_z$. As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current Is will also increase. Their kinetic energy ($W_K = \frac{1}{2}mv^2$) will help in releasing additional carriers through collisions with stable atomic structures. These additional carriers accelerate the ionization process to the point where a high *avalanche* current is established and the *avalanche breakdown* region determined. Once the breakdown voltage is reached, the high reverse current may damage the junction. Hence the reverse voltage across a pn-junction should always less than breakdown voltage. This maximum reverse voltage without destroying the junction is known as *peak inverse voltage (PIV)/ peak reverse voltage (PRV)*. This breakdown voltage is sometimes called *as zener voltage* and the sudden increase in current is known as zener current.

The breakdown voltage of GaAs diodes is about 10% higher those for silicon diodes but after 200% higher than levels for Ge diodes. For GaAs, the reverse saturation current is typically about 1 pA, compared to 10 pA for Si and 1 mA for Ge, a significant difference in levels.

**Temperature Effects:**

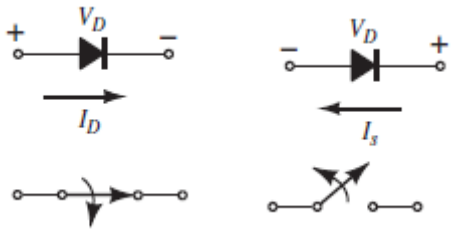
Temperature has a marked effect on the characteristics of a semiconductor diode.

In the *forward-bias region* the characteristics of a silicon diode shift to the left at a rate of 2.5 mV per centigrade degree increase in temperature.

In the *reverse-bias region* the reverse current of a silicon diode doubles for every 10°C rise in temperature. The reverse breakdown voltage of a semiconductor diode will increase or decrease with temperature.

**IDEAL VERSUS PRACTICAL DIODE:**

When a pn-junction is forward biased, it permits a generous flow of charge and when reverse biased, a very small level of current flows. Both conditions are reviewed in Figure below.



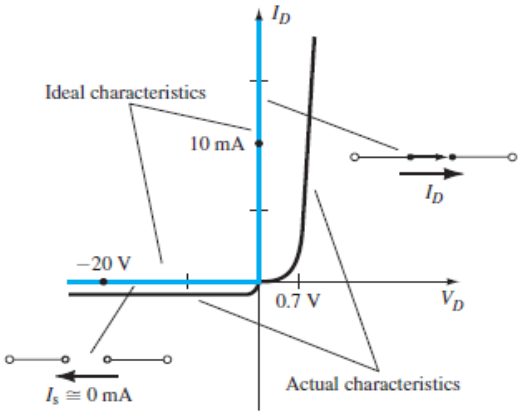

(a) (b)

(Fig. Ideal semiconductor diode: (a) forward biased; (b) reverse-biased.)

The heavy current vector in Fig. (a) matching the direction of the arrow in the diode symbol and the significantly smaller vector in the opposite direction in Fig. (b) representing the reverse saturation current.

This behavior of a semiconductor diode resemblance a mechanical switch. In Fig. (a) the diode is acting like a closed switch permitting a generous flow of charge in the direction indicated. In Fig. (b) the level of current is so small in most cases that it can be approximated as 0 A and represented by an open switch.

That means a semiconductor diode is different from a mechanical switch in the sense that when the switch is closed it will only permit current to flow in one direction. Ideally the resistance of the diode is 0 Ω. In the reverse-bias region its resistance is ∞ and represents an open-circuit equivalent. Such levels of resistance in the forward and reverse-bias regions result in the characteristics of Figure below.




(Fig. Ideal versus actual semiconductor characteristics)

When a switch is closed the resistance between the contacts is assumed to be 0 Ω . At the plot point chosen on the vertical axis the diode current is 5 mA and the voltage across the diode is 0 V. Substituting into Ohm's law results in

$$R_F = \frac{V_D}{I_D} = \frac{0\ V}{5mA} = 0\ \Omega \text{ (short-circuit equivalent)}$$

At any current level on the vertical line, the voltage across the ideal diode is 0 V and the resistance is 0 Ω.

For the horizontal section,

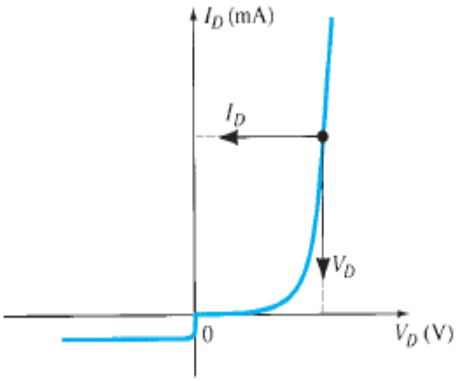
$$R_R = \frac{V_D}{I_D} = \frac{20\ V}{0mA} = \infty\ \Omega \text{ (open-circuit equivalent)}$$

In the reverse-bias region, as reverse saturation current is so small, approximately 0 mA, we have the open-circuit equivalence, assumed as an open switch.

**RESISTANCE LEVELS OF DIODE**

**DC or Static Resistance:**

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of $V_D$ and $I_D$ as shown in Figure below.



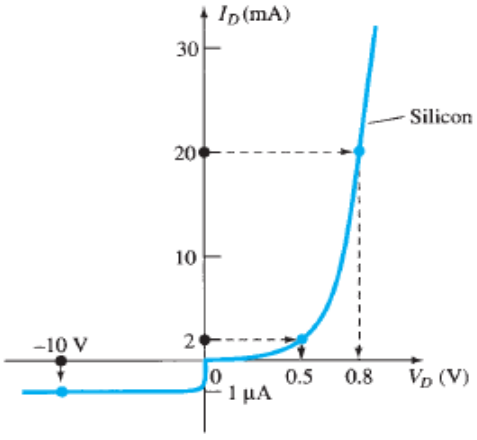

(Fig. Determining the dc resistance of a diode at a particular operating point)

At this operating point resistance of the diode is $R_D = \frac{V_D}{I_D}$ ---------(1)

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high.

**Example:**

Determine the dc resistance levels for the diode of the Figure given below.




(Fig. Example)

At
(a) $\mathrm{I_D} = 2\mathrm{mA}$ (low level)
(b) $\mathrm{I_D} = 20\mathrm{mA}$ (high level)
(c)$V_D$ =-10 V (reverse-biased)

**Answer:**
(a) At $\mathrm{I_D} = 2\mathrm{mA}$, $\mathrm{V_D}$ =0.5 V (from the curve) and

$$\mathrm{R_D} = \frac{\mathrm{V_D}}{\mathrm{I_D}} = \frac{0.5}{2 \times 10^{-3}} = 250\ \Omega$$

(b) At $\mathrm{I_D} = 20\mathrm{mA}$, $\mathrm{V_D}$ =0.8 V (from the curve) and

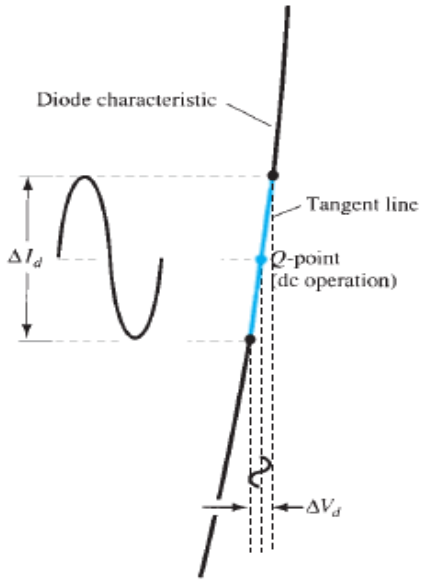
$$\mathrm{R_D} = \frac{\mathrm{V_D}}{\mathrm{I_D}} = \frac{0.8}{20 \times 10^{-3}} = 40\ \Omega$$

(c) $\mathrm{V_D} = -10\mathrm{V}$, $\mathrm{I_D} = -1\mu\mathrm{A}$ (from the curve) and

$$\mathrm{R_D} = \frac{\mathrm{V_D}}{\mathrm{I_D}} = \frac{-10}{-1 \times 10^{-6}} = 10\mathrm{M}\Omega$$

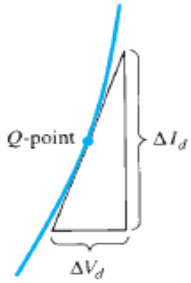
## AC or Dynamic Resistance:

If a sinusoidal input is applied to a diode rather than dc voltage, then this varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Figure below.




(Fig. Defining the dynamic or ac resistance)

With no applied varying signal, the point of operation would be the *Q* -point determined by the applied dc levels. The designation *Q-point* is derived from the word *quiescent* , which means "still or unvarying." A straight line drawn tangent to the curve through the *Q* -point is as shown in Figure below.




(Fig. Determining the ac resistance at a Q-point.)

So a particular change in voltage creates a change in current to determine the *ac* or *dynamic* resistance for this region of the diode characteristics.

AC resistance is $r_d = \frac{\Delta V_d}{\Delta I_d}$ ----------(2)

Δ represents a finite change in the quantity

We have found the dynamic resistance graphically, but there is a basic definition in differential calculus that states:

*The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.*

Equation (2) , as defined by above Figure, is, therefore, essentially finding the derivative of the function at the *Q* -point of operation. If we find the derivative of the general equation for the semiconductor diode with respect to the applied forward bias and then invert the result, we will have an equation for the dynamic or ac resistance in that region. That is, taking the derivative of Eq. with respect to the applied bias will result in

$$\frac{d}{dV_D}(I_D) = \frac{d}{dV_D}\left(I_S(e^{\frac{V_D}{nV_T}} - 1)\right)$$

And $$\frac{dI_D}{dV_D} = \frac{1}{nV_T}(I_D + I_S)$$

after we apply differential calculus.

In general, $I_D \gg I_S$ in the vertical-slope section of the characteristics and

$$\frac{dI_D}{dV_D} \cong \frac{I_D}{nV_T}$$

Flipping the result to define a resistance ratio ( R = V / I ) gives

$$\frac{dV_D}{dI_D} = r_d = \frac{nV_T}{I_D}$$

We know at a temperature of 27°C (common temperature for components in an enclosed operating system), the thermal voltage $V_T$ is

$$V_T = \frac{kT_k}{q}$$

We know T = 273 +°C = 273 + 27 = 300 K

q = 1.6 $\times 10^{-19}$ C and k=1.38$\times 10^{-23}$J/k

Hence $V_T = \frac{kT_k}{q} = \frac{1.38\times10^{-23}\times300}{1.6\times10^{-19}}$= 25.875 mV ≅ 26 mV

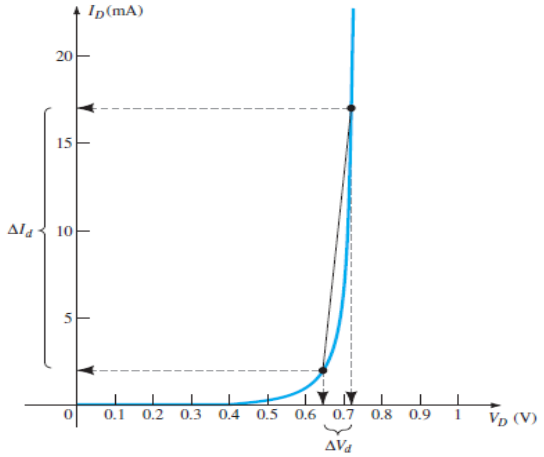
Substituting n =1 and $V_T = 26mV$ results in

$$r_d = \frac{26mV}{I_D}$$ ----------(3)

The equation implies that the dynamic resistance can be found simply by substituting the quiescent value of the diode current into the equation.

## Average AC Resistance

If the input signal is sufficiently large to produce a broad swing such as indicated in Figure below , the resistance associated with the device for this region is called the *average ac resistance* .The average ac resistance is, by definition, the resistance determined by a straight line drawn between the two intersections established by the maximum and minimum values of input voltage. In equation form $r_{av} = \frac{\Delta V_D}{\Delta I_D}$




(Fig. Determining the average ac resistance between indicated limits.)

For the situation indicated by above Figure,

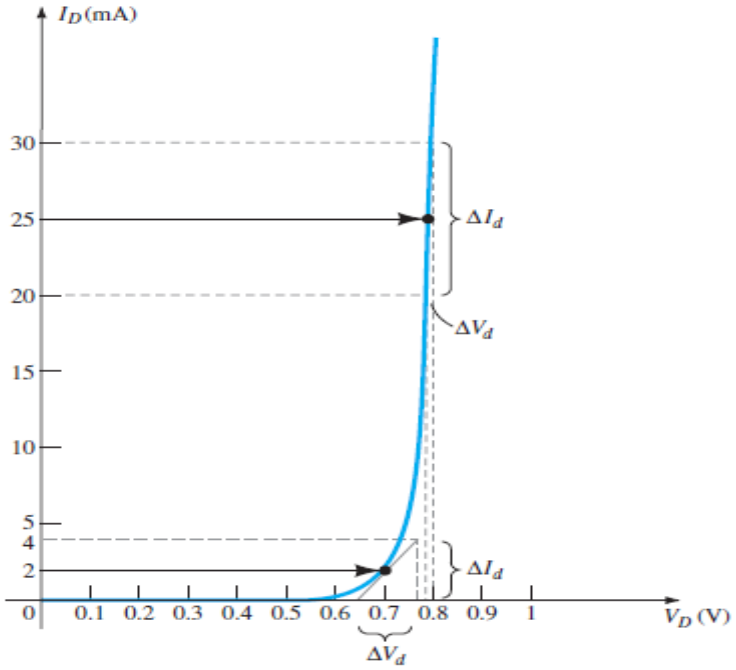
$\Delta I_D$ = 17 mA - 2 mA = 15 mA

and $\Delta V_D$ = 0.725 V - 0.65 V = 0.075 V

with $r_{av} = \frac{\Delta V_D}{\Delta I_D} = 0.075/15x10^{-3} = 5\Omega$

**Example:**

For the characteristics of above Fig.




(Fig. Example)

a. Determine the ac resistance at $I_D = 2mA$

b. Determine the ac resistance at $I_D = 25mA$

c. Compare the results of parts (a) and (b) to the dc resistances at each current level.

**Answer:**

(a) For $I_D = 2mA$ , the tangent line at $I_D = 2mA$ was drawn as shown in Fig. 14 and a swing of 2 mA above and below the specified diode current was chosen.

At $I_D = 4mA, V_D = 0.76\ V$

$I_D = 0mA, V_D = 0.65\ V$

The resulting changes in current and voltage are, respectively,

$\Delta I_D$= 4 mA - 0 mA = 4 mA

and $\Delta V_D = 0.76$ V - 0.65 V = 0.11 V

So ac resistance is is $r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.11}{4\times10^{-3}} = 27.5\Omega$

(b) For $I_D = 25mA$ , the tangent line at $I_D = 25mA$ was drawn as shown in above Figure and a swing of 5 mA above and below the specified diode current was chosen.

At $I_D = 30mA, V_D = 0.8\ V$

$I_D = 20mA, V_D = 0.78\ V$

The resulting changes in current and voltage are, respectively,

$\Delta I_D$= 30 mA - 20 mA = 10 mA

and $\Delta V_D = 0.8$ V - 0.78 V = 0.02 V

So ac resistance is is $r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.02}{10\times10^{-3}} = 2\Omega$

(c) For $I_D$ = 2 mA, $V_D$= 0.7 V and

$$R_D = \frac{V_D}{I_D} = \frac{0.7V}{2mA} = 350\Omega$$

which far exceeds the $r_d$ of 27.5 Ω.

For $I_D$ = 25 mA, $V_D$= 0.79 V and

$$R_D = \frac{V_D}{I_D} = \frac{0.79V}{25mA} = 31.62\Omega$$

which far exceeds the $r_d$ of 2 Ω.

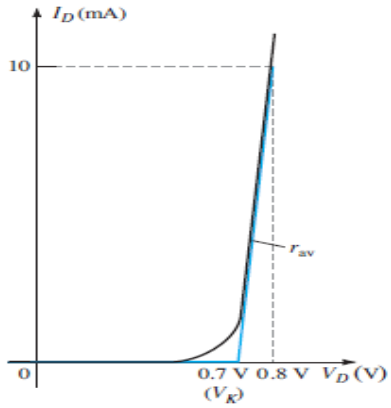
## DIODE EQUIVALENT CIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device or system in a particular operating region.

Once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place.

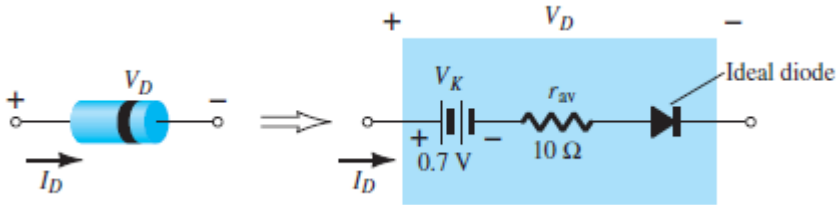
**(a) Piecewise-Linear Equivalent Circuit**

In this method, the characteristic curve of diode is approximated by straight-line segments, as shown in below Figure.




(Fig. Defining the piecewise-linear equivalent circuit using straight-line segments to approximate the characteristic curve)

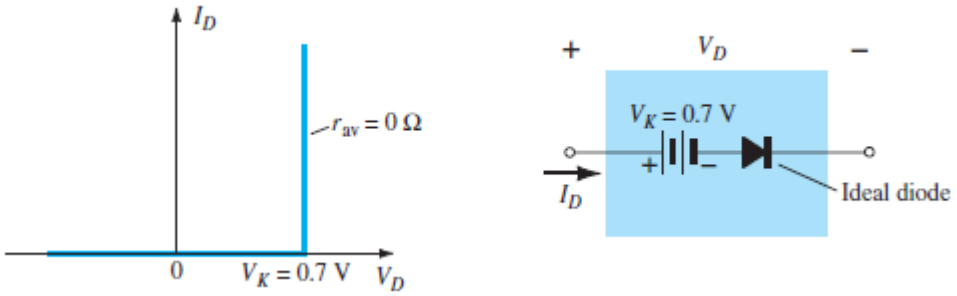
The resulting equivalent circuit is called a *piecewise-linear equivalent circuit.* From the above Figure, it is cleared that the semiconductor diode does not reach the conduction state until $V_D$ reaches $V_T$ (0.7 V for Si, 0.3V for Ge). So in equivalent circuit a battery $V_T$ must be included with the ideal diode. Average resistance $\frac{V_D}{I_D}$ must be included in the Figure below which is at its operating point and denoted as $r_{av}$.




(Fig. Components of the piecewise-linear equivalent circuit)

**(b) Simplified Equivalent Circuit**

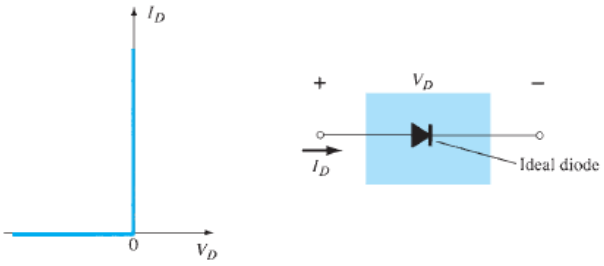
We know the resistance $r_{av}$ is sufficiently small to be ignored in comparison to the other elements of the network. Removing $r_{av}$ from the equivalent circuit is the same as implying that the characteristics of the diode appear as shown in Figure given below.




(Fig. Simplified equivalent circuit for the silicon semiconductor diode)

**(c) Ideal Equivalent Circuit**

If 0.7V of threshold voltage is neglected in comparison to the applied voltage level, the ideal equivalent circuit will be as shown in the Figure given below.

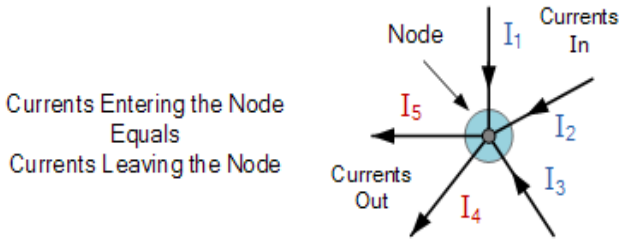



(Fig. Ideal diode and its characteristic)

## KIRCHHOFFS CURRENT (KCL) LAW:

It states that the "*total current or charge entering a junction or node is exactly equal to the charge leaving the node as it has no other place to go except to leave, as no charge is lost within the node*".

In other words the algebraic sum of ALL the currents entering and leaving a node must be equal to zero, $I_{(exiting)} + I_{(entering)} = 0$. This idea by Kirchhoff is commonly known as the **Conservation of Charge**.
Example:




Here, the three currents entering the node, $I_1$, $I_2$, $I_3$ are all positive in value and the two currents leaving the node, $I_4$ and $I_5$ are negative in value. Then this means we can also rewrite the equation as;

$$I_1 + I_2 + I_3 + (-I_4) + (-I_5) = 0$$

i.e

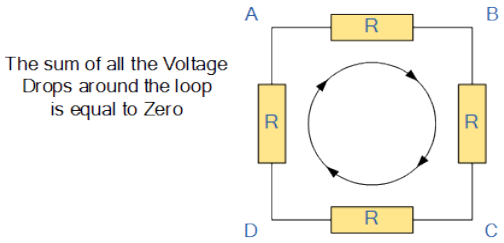
$$I_1 + I_2 + I_3 - I_4 - I_5) = 0$$

The term **Node** in an electrical circuit generally refers to a connection or junction of two or more current carrying paths or elements such as cables and components. Also, for current to flow either in or out of a node a closed-circuit path must exist. Kirchhoff's current law is used when analyzing parallel circuits.

## KIRCHHOFFS VOLTAGE (KVL) LAW:

It's states that "*in any closed loop network, the total voltage around the loop is equal to the sum of all the voltage drops within the same loop*" which is also equal to zero. In other words

the algebraic sum of all voltages within the loop must be equal to zero. This idea by Kirchhoff is known as the **Conservation of Energy**.



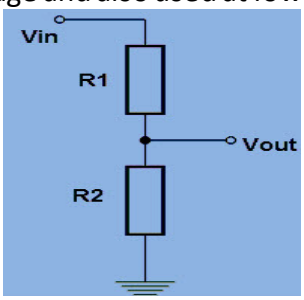

$V_{AB} + V_{BC} + V_{CD} + V_{DA} = 0$

Starting at any point in the loop continue in the **same direction** noting the direction of all the voltage drops, either positive or negative, and returning back to the same starting point. It is important to maintain the same direction either clockwise or anti-clockwise or the final voltage sum will not be equal to zero. We can use Kirchhoff's voltage law when analyzing series circuits.

## VOLTAGE DIVISION RULE

The statement of the **rule** is "The **voltage** is divided between two series resistors in direct proportion to their resistance".

In electronics, the voltage divider rule is used to change a large voltage into a small voltage. The best example for voltage divider is two resistors are connected in series. When the i/p voltage is applied across the pair of the resistor and the o/p voltage will appear from the connection between them. Generally, these dividers are used to reduce the magnitude of the voltage or to create reference voltage and also used at low frequencies as a signal attenuator.




Voltage Divider Rule

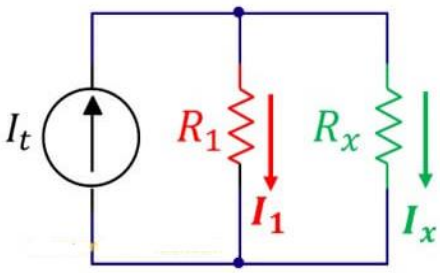
$V_{in}$ is the input voltage. $R_1$ and $R_2$ are two series resistors. According to this rule $V_{out} = \frac{R_2}{R_1+R_2} V_{in}$

## CURRENT DIVISION RULE

In electronics a **current divider** is a simple linear circuit that produces an output current ($I_X$) that is a fraction of its input current ($I_T$). **Current division** refers to the splitting of current between the branches of the divider. The currents in the various branches of such a circuit will always divide in such a way as to minimize the total energy expended.

To be specific, if two or more impedances are in parallel, the current that enters the combination will be split between them in inverse proportion to their impedances (according to Ohm's law). It also follows that if the impedances have the same value the current is split equally.

A general formula for the current $I_X$ in a resistor $R_X$ that is in parallel with a combination of other resistors of total resistance $R_t$ is:




$$I_x = \frac{R_t}{R_x + R_t} \times I_t$$

where $R_t = R_1 \, II \, R_x$

here $I_T$ is the total current entering the combined network of $R_X$ in parallel with $R_T$. Notice that when $R_t$ is composed of a parallel combination of resistors, say $R_1$, $R_2$, ... *etc.*, then the reciprocal of each resistor must be added to find the total resistance $R_t$.

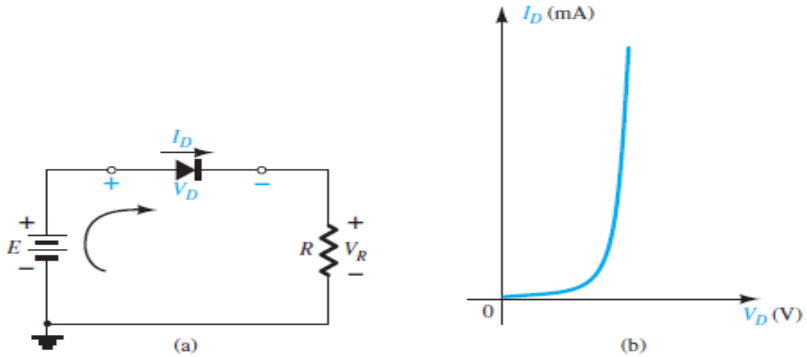
**Applications of Semiconductor Diode**

**Objective:**

- Understand the concept of load-line analysis and how it is applied to diode networks, Diode as Switch (ON, OFF Switch)
- Become familiar with the use of equivalent circuits to analyze series, parallel, and Series-parallel diode networks.

**Load Line Analysis:**

The circuit of Fig. shown below is the simplest of diode configuration. It will be used to describe the
analysis of a diode circuit using its actual characteristics.

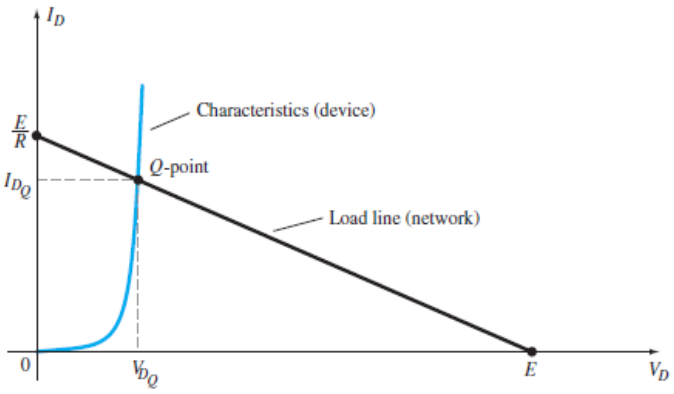



*Series diode configuration: (a) circuit; (b) characteristics.*

A plot of the current $I_D$, versus the voltage drop across the diode $V_D$, will yield a straight line, called the "Load Line", of possible values of current flow in the circuit. We form the line by applying the KVL,

$$E - V_D - V_R = 0$$
$$E = V_D + V_R$$
$$E = V_D + I_D R$$

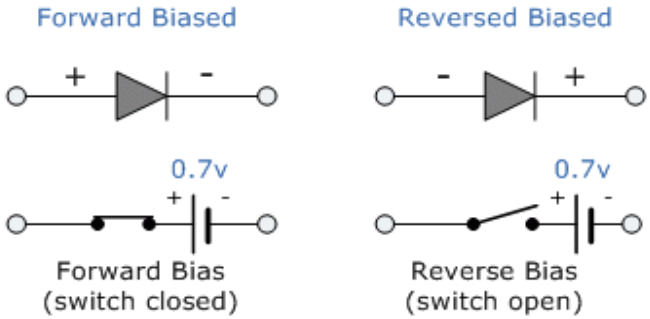
$I_D$= 0 at $V_D$ = E and that $I_D$ = E/R at $V_D$ = 0 as shown below. The point of intersection the device characteristics curve and the load line is called as operating point (Q-point).
The following figure shows both load line and Q-point,




*Drawing the load line and finding the point of operation (Q-point)*

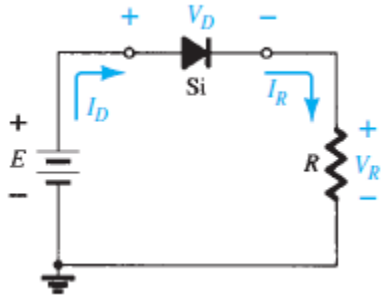
**Diode as Switch (ON, OFF Switch):**

Diodes can perform switching and digital logic operations. When diode is forward biased, it exhibits very low impedance (ideally short circuited) and behaves as ON switch. When diode is Reverse biased, it exhibits very high impedance (ideally open circuited) and behaves as OFF switch. Thus, it serves as a switch. The fig. shown below represents diode as switch.

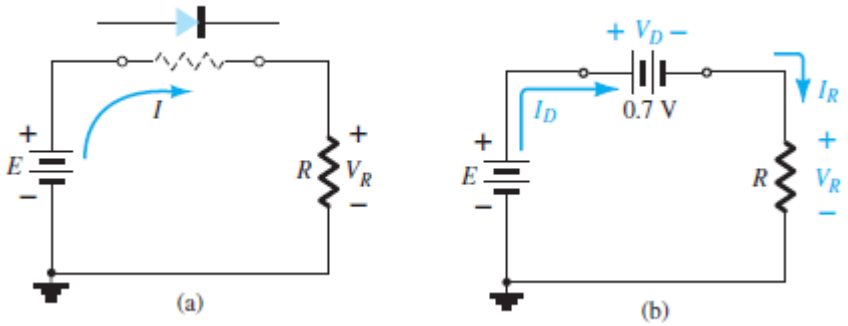



**Series Diode Configurations:**

The series circuit using diode consists up of diode (diodes) in series with the resistive load and Series diode configuration is shown below figure.



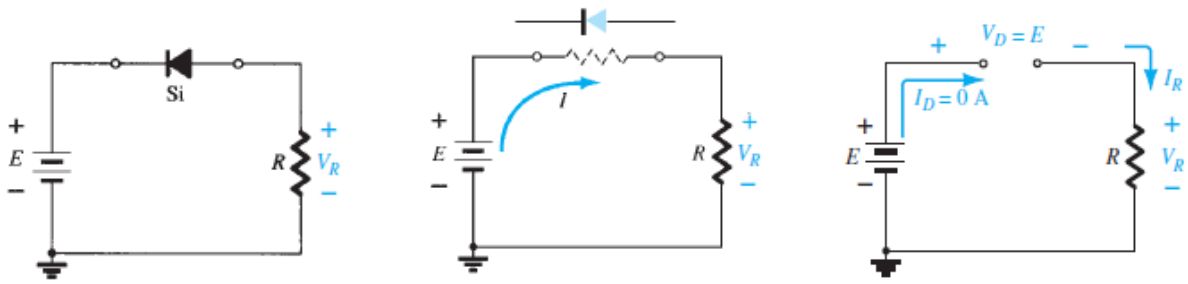

The state of the diode is first determined by mentally replacing the diode with a resistive element as shown in figure below.




If the resulting direction of I is a match with the arrow in the diode symbol, then the diode is in the "on" state. The network is then redrawn as shown in above fig. b with the appropriate equivalent model for the forward-biased silicon diode.
The resulting voltage and current levels are the following:

$$V_D = 0.7v$$
$$V_R = E - 0.7$$
$$I_D = I_R = \frac{V_R}{R}$$

If the resulting direction of I does not match with the arrow in the diode symbol, then the diode is in the "OFF" state. The network is then redrawn as shown in below fig. b with the appropriate equivalent model for the forward-biased silicon diode.




*Reversing the diode of the above Fig.* *Determining the state of the diode* *Substituting the equivalent model*

Due to the open circuit, the diode current is 0 A and the voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = 0v$$

**Parallel and Series–Parallel Configurations:**
The methods applied in Series diode configuration can be extended to the analysis of parallel and series–parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

## APPLICATION OF SEMICONDUCTOR DIODE

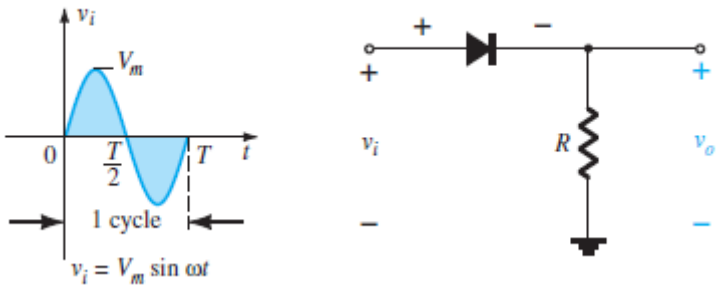
### (1) Diode as a Rectifier

The electrical power is generated, transmitted and distributed in a.c. form, means at the mains, an alternating voltage is available. But most of the electronic circuits need d.c. voltage for their operation. Therefore, now-a-days almost all the equipment require a circuit known as rectifier which converts a.c. voltage of main supply into d.c. voltage. It is a part of power supply unit. Rectifiers are classified into two types:

(1) Half wave rectifier
(2) Full wave rectifier

(1) Half wave rectifier-

In half wave rectification, when ac supply is applied at the input, only +ve half cycle appear across the load, whereas –ve half cycle is suppressed.



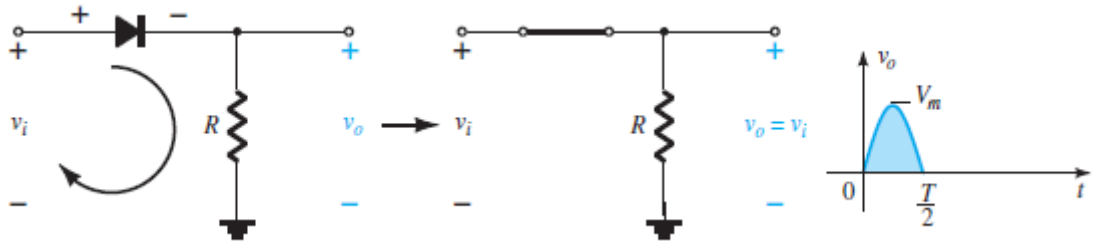

**Construction:**

For rectification only one crystal diode is used. It is connected in the circuit as shown in the above Figure. The a.c. supply to be rectified is generally given through a transformer. The transformer is used to step down or step up the main supply voltage as per requirement. It also isolates the rectifier circuit from power lines and thus reduces the risk of electric shock.

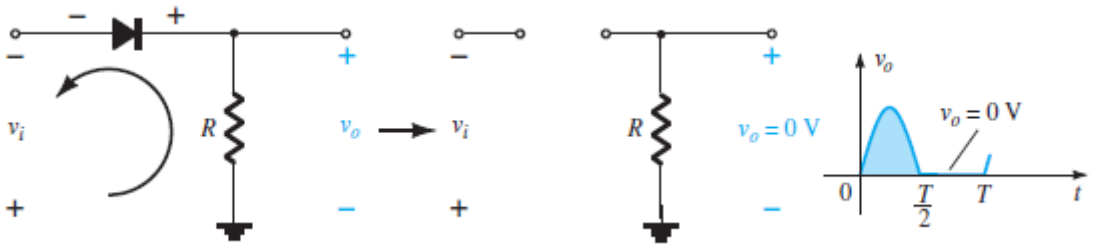
**Operation:**

When a.c supply is switched on, during positive half cycle, the upper terminal is positive w.r.t lower and the diode is forward biased. Therefore, it conducts and the current $i$ flows through the load resistor $R_L$. This current varies in magnitude as shown in the below Fig. Thus, a positive half cycle of output voltage $v_{out} = iR_L$ appears across the load resistor as shown in below Fig. During negative half cycle, the upper terminal is negative w.r.t lower and the diode

is reversed biased. Therefore, it does not conduct and no current and no voltage appears across the load resistor $R_L$.




(Conduction Region 0 to T/2)




(Conduction Region T/2 to T)

**Efficiency of half wave rectifier:**

The ratio of d.c. power output to the a.c. power input is called as rectifier efficiency.

Mathematically,

Rectifier Efficiency $\eta = \frac{\text{d.c. power output}}{\text{a.c. power input}}$

For half wave rectifier, let the voltage appears across the secondary of power transformer be $v = v_m \sin\theta$, forward resistance of diode be $r_f$ and load resistance be $R_L$.

Current flows through the load resistor only during positive half cycle when the diode is forward biased. During negative half cycle, the diode is reversed biased and no current flows through the circuit.

The instantaneous value of current during conduction period is

$$i = \frac{v}{R_L + r_f} = \frac{v_m \sin\theta}{R_L + r_f}$$

The current is maximum when $\sin\theta = 1$.

Hence $I_m = \frac{v_m}{R_L + r_f}$, so $i = I_m \sin\theta$

The d.c. power output $P_{dc} = I_{dc}^2 R_L = I_{av}^2 R_L$

Where $I_{av} = \int_0^{\pi} \frac{i\, d\theta}{2\pi}$

$$= \frac{1}{2\pi}\int_0^{\pi} I_m \sin\theta\, d\theta$$

$$= \frac{I_m}{2\pi}[-\cos\theta]_0^{\pi}$$

$$= \frac{I_m}{2\pi} \times 2 \quad = \frac{I_m}{\pi}$$

Hence d.c. power output $P_{dc} = I_{dc}^2 R_L$

$$= \left(\frac{I_m}{\pi}\right)^2 R_L$$

The a.c. power input $P_{ac} = I_{rms}^2 (R_L + r_f)$

Where $I_{rms}^2 = \frac{\int_0^{\pi} i^2 d\theta}{2\pi}$

Hence $I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\theta\, d\theta}$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi}\left(\frac{1-\cos 2\theta}{2}\right) d\theta} \quad = \frac{I_m}{2}$$

Hence a.c. power input $P_{ac} = I_{rms}^2 (R_L + r_f)$

So, rectifier efficiency $\eta = \frac{\text{d.c. power output}}{\text{a.c. power input}} = \frac{P_{dc}}{P_{ac}}$

$$= \frac{\left(I_m/\pi\right)^2 R_L}{\left(I_m/2\right)^2 (R_L + r_f)}$$

$$= \frac{0.406}{1 + \frac{r_f}{R_L}}$$

If $r_f$ is neglected w.r.t $R_L$, then

$$\eta_{max} = 40.6\%$$

The result shows that the half wave rectifier can convert maximum 40.6% of a.c. power into d.c. power. The remaining 59.4% power is lost in the circuit. In fact, 50% power in –ve half cycle is not converted and the remaining 9.4% is lost in the circuit.

D.C. output voltage:

$$v_{dc} = I_{dc} R_L = I_{av} R_L$$

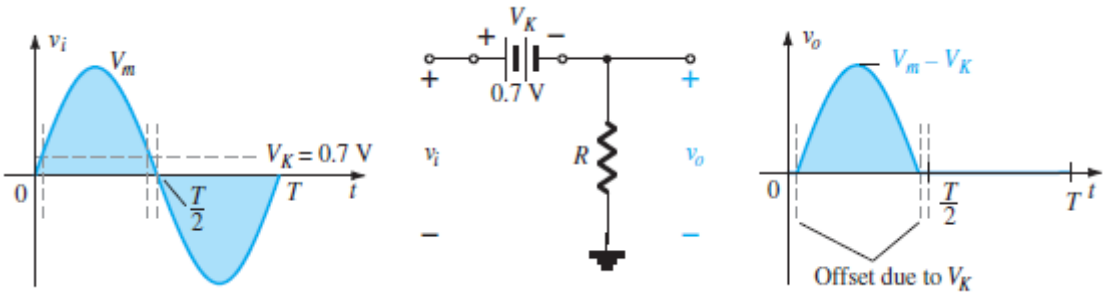
$$= \frac{I_m}{\pi} R_L = \frac{v_m}{\pi (R_L + r_f)} R_L$$

$$= \frac{v_m}{\pi(1+r_f/R_L)} R_L$$

At no load, i.e. $R_L = \infty$

$$v_{dc} = \frac{v_m}{\pi}$$

The effect of using a Si diode with $V_k$ as 0.7V is shown below.




For levels of $v_i$ less than 0.7 volts, the diode is still in an open circuit state and $v_o$ is 0 volts as shown in fig. when conducting, the difference between $vo$ and $v_i$ is a fixed level of $v_k = 0.7$volts and $v_0 = v_i - v_k$.

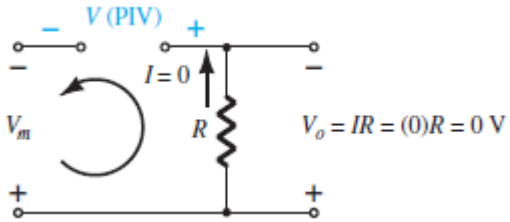
Hence d.c. output voltage becomes

$$v_{dc} = \frac{Vm-Vk}{\pi} = 0.318\ (v_m - vk)$$

**PIV (Peak Inverse Voltage):**

During negative half cycle when diode is reverse biased, the maximum value of the voltage coming across the diode is known as peak inverse voltage (PIV).

The required PIV rating for the half wave rectifier can be determined from the Fig., which display the reverse biased diode of the following Fig. with maximum applied voltage.




Applying Kirchoff's voltage Law,

$$v_m - PIV = 0$$

Hence $PIV_{rating} \geq v_m$

**Ripple Factor:**

In a rectifier output, the ratio of r.m.s value of a.c. component (or ripple) to the d.c. component is known as ripple factor.

$$\text{Ripple factor} = \frac{\text{r.m.s value of a.c. component}}{\text{value of d.c component}}$$

This factor decides the effectiveness of a rectifier.

Mathematically,

$$\text{Ripple factor} = \frac{I_{ac}}{I_{dc}}$$

$$= \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

For half wave rectifier, $I_{rms} = \frac{I_m}{2}$ and $I_{dc} = \frac{I_m}{\pi}$

Hence $(\text{ripple factor})_{\text{half wave rectifier}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

$$= \sqrt{\left(\frac{\frac{I_m}{2}}{\frac{I_m}{\pi}}\right)^2 - 1} \quad = \sqrt{(1.57)^2 - 1}$$

$$= 1.21$$

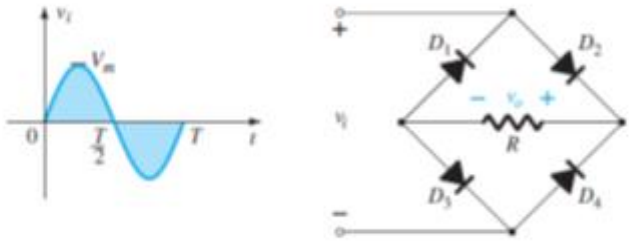
From this it is cleared that in the output of a half wave rectifier, the ac component exceeds the dc component. Means the output of a half wave rectifier contains more ripples. Hence it is rarely applied.

**<u>Full Wave Rectifier</u>**

Full wave rectifiers have some fundamental advantages over their half wave rectifier counterparts. The average (DC) output voltage is higher than for half wave, the output of the full wave rectifier has much less ripple than that of the half wave rectifier producing a smoother output waveform.

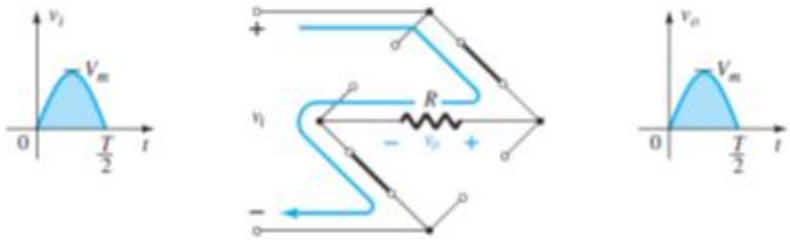
1. **Bridge Network**

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification.* The most familiar network for performing such a function appears in Fig. with its four diodes in a *bridge* configuration. During the period *t* _ 0 to *T* >2 the polarity of the input is as shown in Fig. The resulting polarities across the ideal diodes are also shown in Fig. to reveal that *D* 2 and *D* 3 are conducting, whereas *D* 1 and *D* 4 are in the "off" state. The net result is the configuration of Fig., with its indicated current and polarity across *R.* Since the diodes are ideal, the load voltage is *vo* = *vi*, as shown in the same figure.




*Full-wave bridge rectifier.*

*Network for the period $0 \rightarrow T/2$ of the input voltage $v_i$*




*Conduction path for the positive region of $v_i$*

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

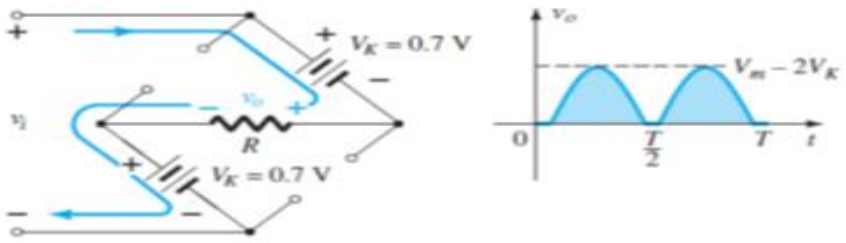
$$V_{dc} = 2(o.318V_m)$$

$$or \qquad V_{dc} = 0.616V_m$$

If silicon rather than ideal diodes are employed as shown in Fig., the application of Kirchhoff's voltage law around the conduction path results in

$$V_i - V_k - V_o - V_k = 0$$

$$V_o = V_i - 2V_k$$




*Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.*

The peak value of the output voltage $v_o$ is therefore

$$V_{o_{max}} = V_m - 2V_K$$

For situations where $V_m \gg 2V_K$, the following equation can be applied for the average value with a relatively high level of accuracy:

$$V_{dc} \cong 0.636(V_m - 2V_K)$$

Then again, if $V_m$ is sufficiently greater than $2V_K$, then Eq. (2.10) is often applied as a first approximation for $V_{dc}$.

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$$V_{dc} \cong 0.636(V_m - 2V_K)$$

Then again, if $V_m$ is sufficiently greater than $2V_K$, then Eq. (2.10) is often applied as a first approximation for $V_{dc}$.

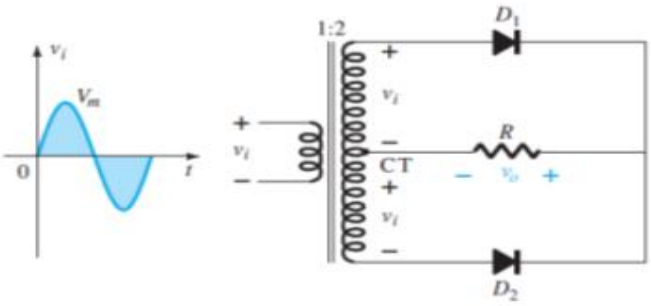
**PIV** The required PIV of each diode (ideal) can be determined from Fig. 2.59 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across $R$ is $V_m$ and the PIV rating is defined by

$$\text{PIV} \geq V_m$$

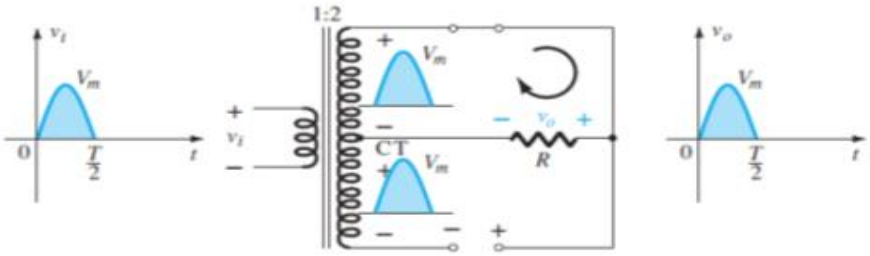
full-wave bridge rectifier

**Center-Tapped Transformer**

A second popular full-wave rectifier appears in Fig. with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of *v i* applied to the primary of the transformer, the network will appear as shown in Fig. 2.61 with a positive pulse across each section of the secondary coil. *D* 1 assumes the short-circuit equivalent and *D* 2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig.

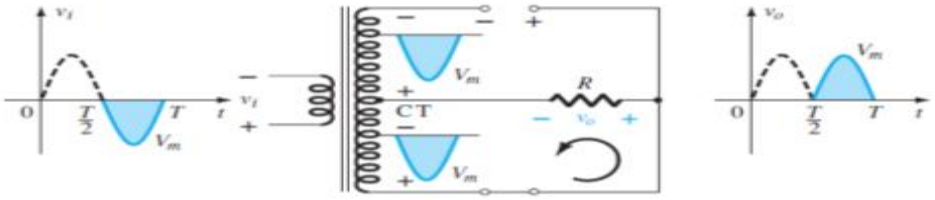



*Center-tapped transformer full-wave rectifier.*




*Network conditions for the positive region of $v_i$.*

During the negative portion of the input the network appears as shown in Fig, reversing the roles of the diodes but maintaining the same polarity for the voltage across the load resistor *R.* The net effect is the same output as that appearing in Fig. with the same dc levels.




*Network conditions for the negative region of $v_i$.*

**PIV** The network of Fig. 2.63 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and $V_m$ as established by the adjoining loop results in

$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

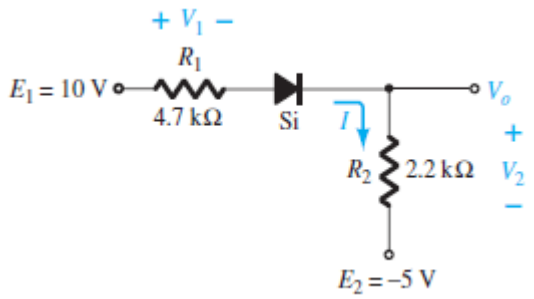
and

$$\boxed{\text{PIV} \geq 2V_m}$$ CT transformer, full-wave rectifier

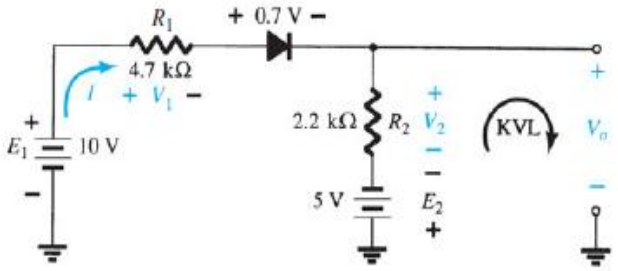
**Numerical Problem Solving:**

- Problem of Series, Parallel, Series–Parallel Diode Configurations
- Problem of Rectifier

**Q-1**. Determine $I, V_1, V_2, and\ V_0$ for the series dc configuration of Fig. shown below.




**Sol:** The sources are drawn and the current direction indicated as shown in Fig. The diode is in the "on" state and the notation appearing in the above Fig. is included to indicate this state. Note that the "on" state is noted simply by the additional $V_D = 0.7V$ on the figure.




The resulting current through the circuit and the voltages are

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{14.3V}{6.9K} \cong 2.07mA$$

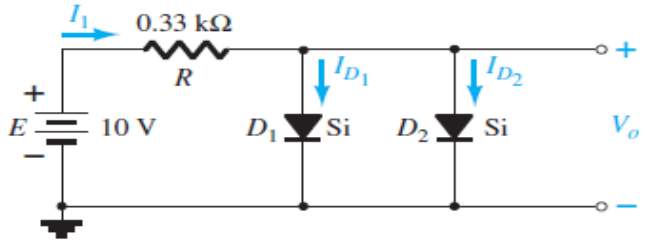
$V_1 = IR_1 = 9.73V$
$V_2 = IR_2 = 4.55V$

Applying KVL to the outer loop,

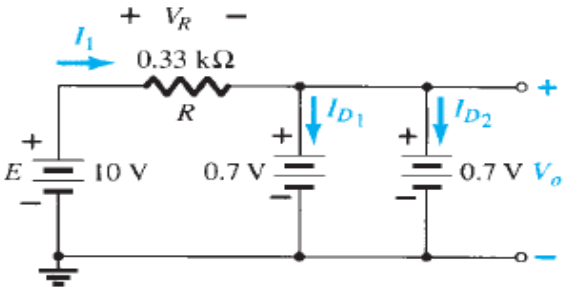
$$-E_2 + V_2 - V_0 = 0$$

$$V_0 = 4.55V - 5V = -0.45V$$

**Q.2** Determine $V_0, I_1, I_{D1}, and\ I_{D2}$ for the circuit shown below.




**Sol:** By E=10v, both the diodes are forward bias and replaced by their equivalent Model as shown below




$$V_o = 0.7V$$

The current $I_1$ is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = \mathbf{28.18\text{ mA}}$$

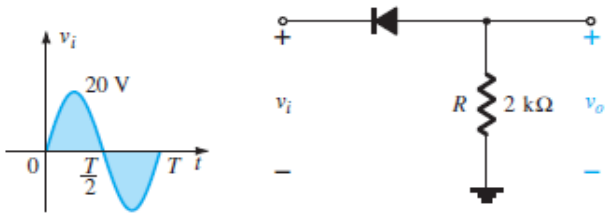
Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = \mathbf{14.09\text{ mA}}$$

**Q.3**

a. Sketch the output $V_0$ and determine the dc level of the output for the network of Fig. shown below

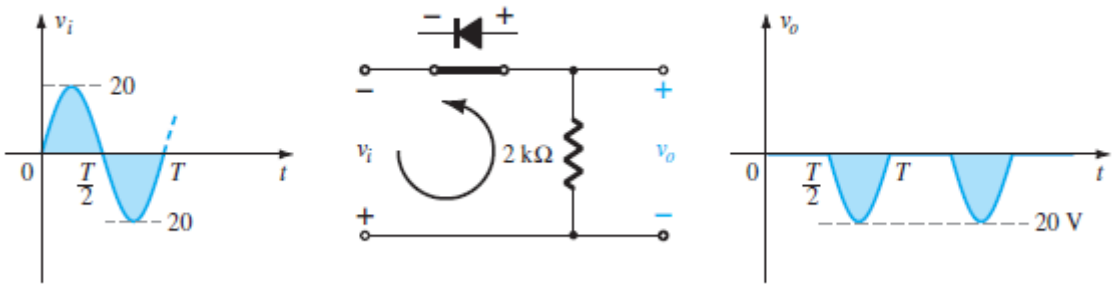
b. Repeat part (a) if the ideal diode is replaced by a silicon diode.




**Sol:**

(a) In this situation the diode will conduct during the negative part of the input and $V_0$ will appear as shown in figure below. For the full period, the dc level is given as

$$V_{dc} = -0.318V_m = -0.318 \times 20V = -6.36V$$

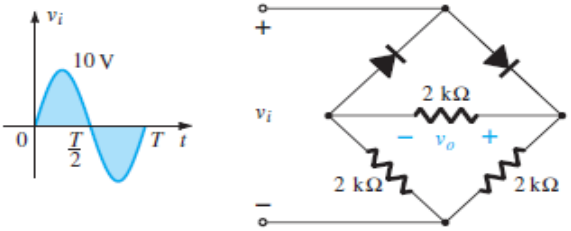



(b) For a silicon diode,

$$V_{dc} = -0.318(V_m - 0.7) = -0.318 \times 19.3V = -6.14V$$

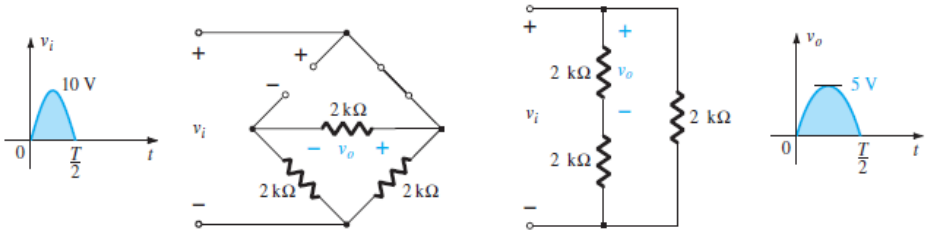
The resulting drop in dc level is 0.22 V, or about 3.5%.

**Q.4** Determine the output waveform for the network shown below and calculate the output dc level and the required PIV of each diode.



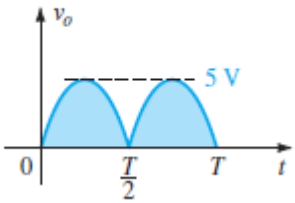

**Sol:**

For the positive half cycle of the input voltage. Redrawing the network results as




$$V_o = \frac{1}{2}(10V) = 5V$$

For the both half cycle of the input, the output $V_o$ appears as shown below



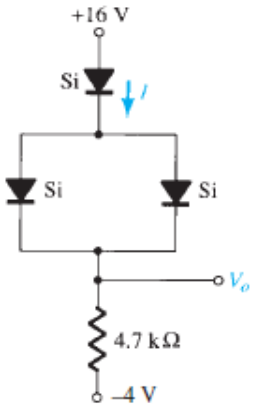

The dc output voltage is given by

$$V_o = 0.636X5V = 3.18V$$

The PIV voltage is given by

$$V_{PIV} = 5V$$

**Q.5** Determine $V_o$ and I for the network shown below.




**Sol:**

Because of +16V and -4V are connected across the P-side and N-side of diodes, all three diodes will be forward biased and replaced by 0.7V each. So the output voltage $V_o$ is given by

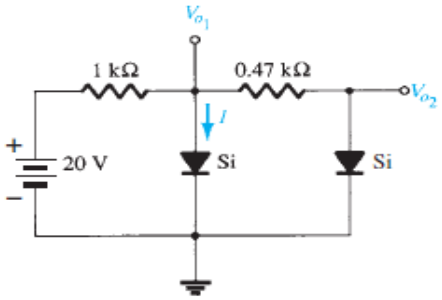
$$V_o = 16 - 0.7 - 0.7 = 14.6V$$

The current in the network I is given by

$$I = \frac{V_o - (-4)}{4.7} mA = \frac{18.6}{4.7} mA = 3.957mA$$

**Q.6**

Determine $\mathrm{V_{o1}}, \mathrm{V_{o2}}$, and I for the network of Fig. shown below.




Sol:

Because of 20V both Si diodes will be forward biased, and replaced by 0.7V each.

$$\mathrm{V_{o1}} = 0.7\mathrm{V} \text{ and } \mathrm{V_{o2}} = 0.7\mathrm{V}$$

The current through 0.47KΩ is given by 0A (as $\mathrm{V_{o1}} = 0.7\mathrm{V}$ and $\mathrm{V_{o2}} = 0.7\mathrm{V}$) and the current I is given by

$$I = \frac{20 - 0.7}{1K} = 19.3mA$$

## Zener Diode

**Objective:**

- Understand the concept of Breakdown Mechanism
- Study of V-I Characteristics of Zener diode

- Familiar with the equivalent Model of Zener diode

**Junction Breakdown Mechanism:**

Consider the I-V characteristics of a pn junction in reverse bias, as shown in fig. shown below. There is initially a small reverse saturation current due to thermally generated electron and holes in the depletion region. This current is called drift current, since this is due to movement of the thermally generated carriers under the applied electric field. With increase in voltage there is a particular value, called the breakdown voltage, beyond which the current increases rapidly. This is called junction breakdown. There are two main mechanisms of junction breakdown, depending on the dopant concentration levels.

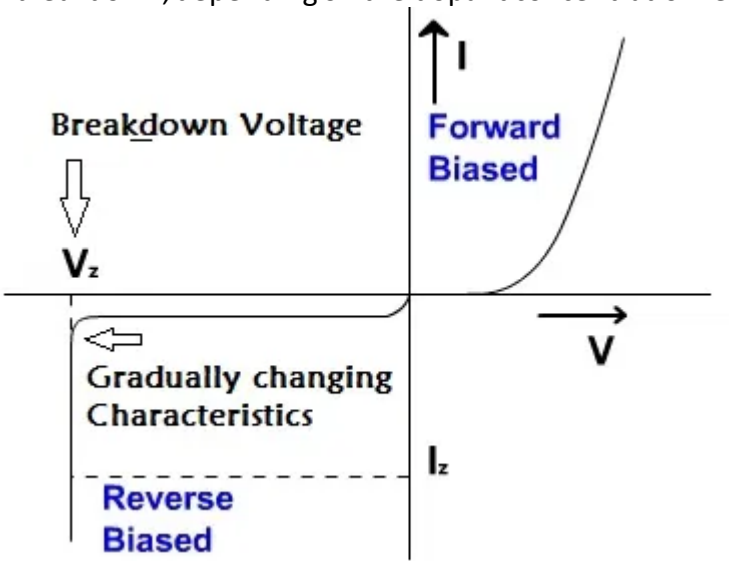



Fig. V-I characteristics heavily dopped diode

**Avalanche breakdown:**

The avalanche breakdown is observed in the Zener Diodes having Vz having than 8 V. In the reverse biased condition, the conduction will take place only due to the minority carriers. As we increase the reverse voltage applied to the Zener diode, these minority carriers tend to accelerated. Therefore, the kinetic energy associated with them increases. While travelling, these accelerated minority carriers will collide with the stationary atoms and impart some of the kinetic energy to the valence electrons present in the covalent bonds.

Due to this additionally acquired energy, these valence electrons will break their covalent bonds and jump into the conduction bond to become free conduction. Now these newly generated free electrons will get accelerated. They will knock out some more valence electrons by means of collision. This phenomenon is called as carrier multiplication.

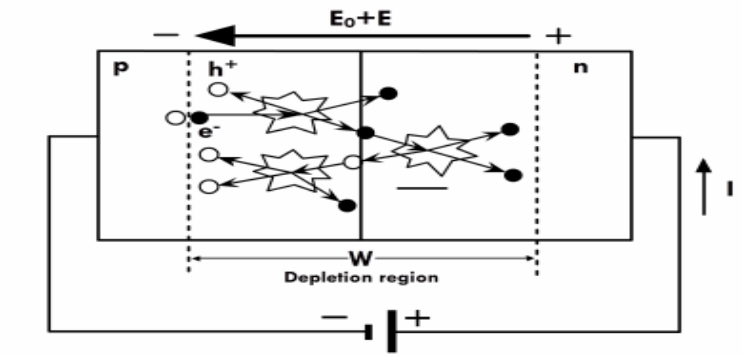



*Fig. Avalanche breakdown in a lightly doped pn junction*

**Zener breakdown:**

The Zener Breakdown is observed in the Zener diodes having Vz less than 5V or between 5 to 8 volts. When a reverse voltage is applied to a Zener diode, it causes a very intense electric field to appear across a narrow depletion region. Such an intense electric field is strong enough to pull some of the valence electrons into the conduction band by breaking their covalent bonds. these electrons then become free electrons which are available for conduction. A large number of such free electrons will constitute a large reverse current through the Zener diode and breakdown is said to have occurred due to the Zener effect.

**VI characteristics of Zener diode:**

The VI characteristics of a Zener diode are shown in the below figure. When a forward biased voltage is applied to the Zener diode, it works like a normal diode. However, when a reverse biased voltage is applied to the Zener diode, it works in a different manner.

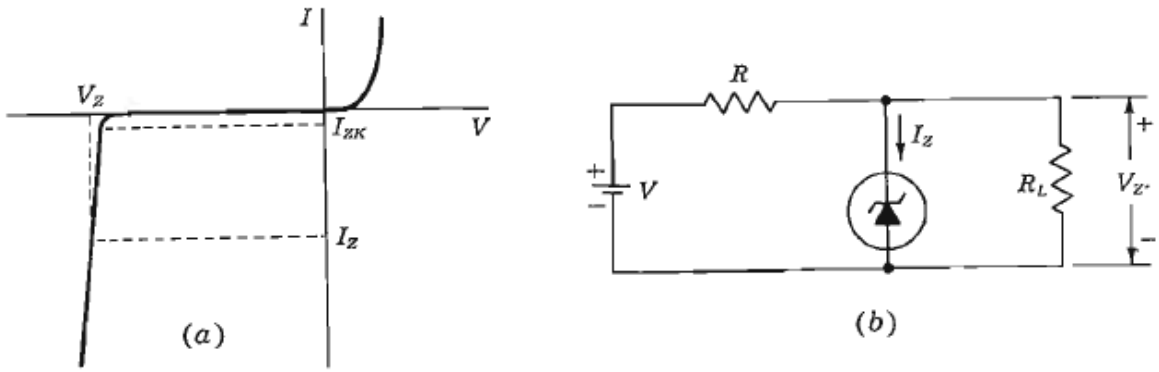



Fig. (a) *The V-I Characteristics of Zener diode* (b*) A circuit in which such a diode is used as voltage regulator*

**Equivalent Model of Zener diode:**

The analysis of networks employing Zener diodes is quite similar to the analysis of semiconductor diodes. First the state of the diode must be determined, followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Fig. shown below reviews the approximate equivalent model for each region of a Zener diode assuming the straight-line approximations at each break point.

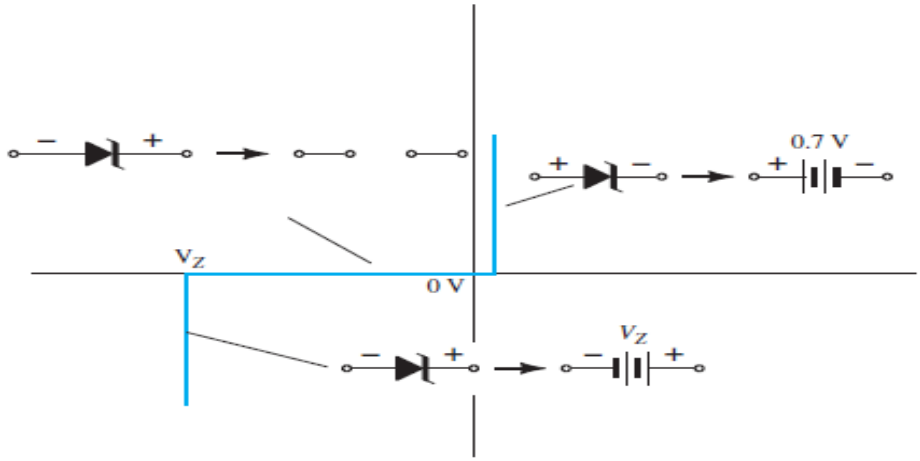



Fig. *Approximate equivalent model for the Zener diode in the three possible regions of application.*

**Application of Zener Diode:**

- Zener diode as Voltage Regulator
- Variable $V_i$ and $R_L$ Fixed
- Fixed $V_i$ , Variable $R_L$
- Problems on Zener diode

**Zener diode as Voltage Regulator:**

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered. The analysis provides an excellent opportunity to become better acquainted with the response of the Zener diode to different operating conditions. The basic configuration appears in Fig. shown below. The analysis is first for fixed quantities, followed by a fixed supply voltage and a variable load, and finally a fixed load and a variable supply.

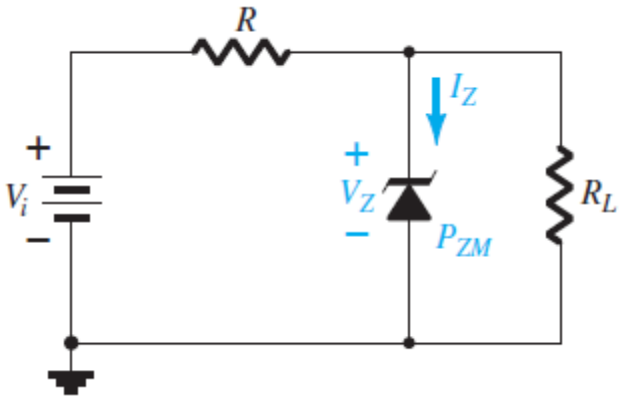
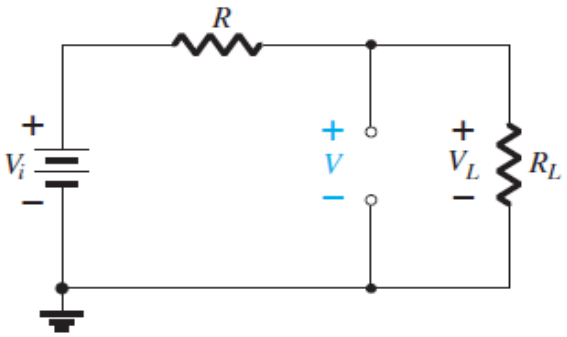



Fig. Basic Voltage Regulator circuit.

**Case-I: $V_i$ and R Fixed**

The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

Step 1: Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit. The circuit is as shown below,




$$V = V_L = \frac{R_L V_i}{R + R_L}$$

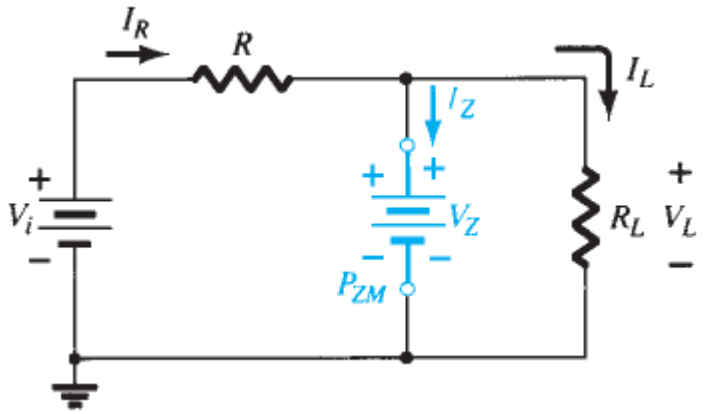
If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted.

If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

Step 2: Substitute the appropriate equivalent circuit and solve for the desired unknowns.

**Case-II: $V_i$ variable and R Fixed and Case: III $V_i$ Fixed and R variable**

For Zener diode as voltage regulator, diode must be in breakdown and replace the zener diode as its equivalent model as below fig. and apply KVL and KCL to calculate unknown quantities.




The Zener diode current must be determined by an application of Kirchhoff's current law.

$$I_R = I_Z + I_L$$

Where $I_L = \frac{V_L}{R_L}$ and $I_R = \frac{V_i - V_L}{R}$

The power dissipated by the Zener diode is determined by

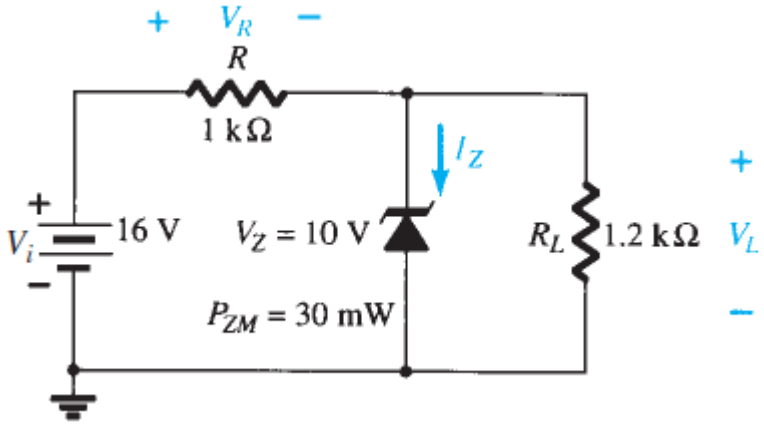
$$P_Z = V_Z I_Z$$

$P_Z$ must be less than the $P_{ZM}$ specified for the device.

**Numerical Problem of Zener diode:**

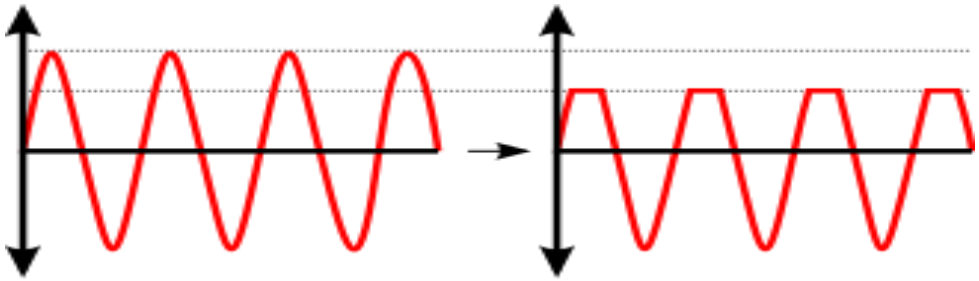
**Q.**(a) For the Zener diode network of Fig. shown below, determine $V_L$ , $V_R$, $I_Z$, and $P_Z$.

(b) Repeat part (a) with RL = 3 kΩ




## Clippers

A clipping circuit or a clipper is a device used to 'clip' the input voltage to prevent it from attaining a value larger than a predefined one. As you can see in the picture below this device cuts off the positive or negative peak value of a cycle.



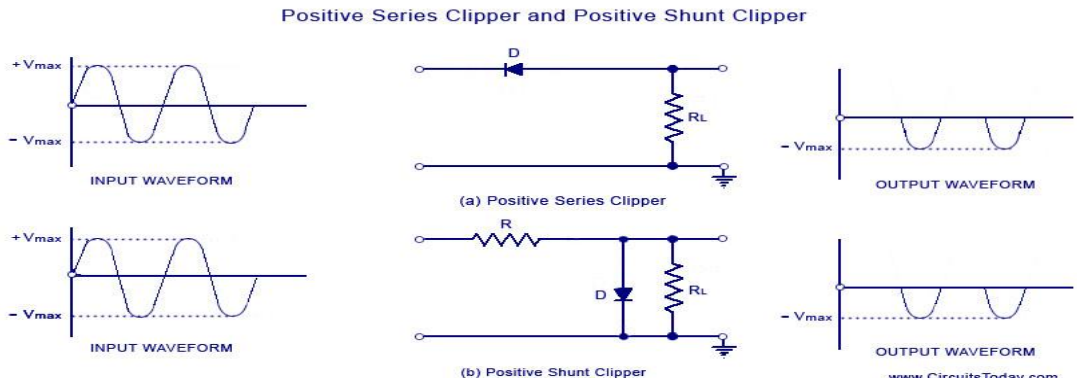
The basic components required for a clipping circuit are – an ideal diode and a resistor. In order to fix the clipping level to the desired amount, a dc battery must also be included. A When the diode is forward biased, it acts as a closed switch, and when it is reverse biased, it acts as an open switch. Different levels of clipping can be obtained by varying the amount of voltage of the battery and also interchanging the positions of the diode and resistor. Depending on the features of the diode, the positive or negative region of the input signal is "clipped" off and accordingly the diode clippers may be positive or negative clippers.

**There are two general categories of clippers: series and parallel (or shunt). The series configuration is defined as one where a diode is in series with the load, while the shunt clipper has the diode in a branch parallel to the load.**

## 1. Positive Clipper and Negative Clipper

*Positive Diode Clipper*

In a positive clipper, the positive half cycles of the input voltage will be removed. The circuit arrangements for a positive clipper are illustrated in the figure given below.



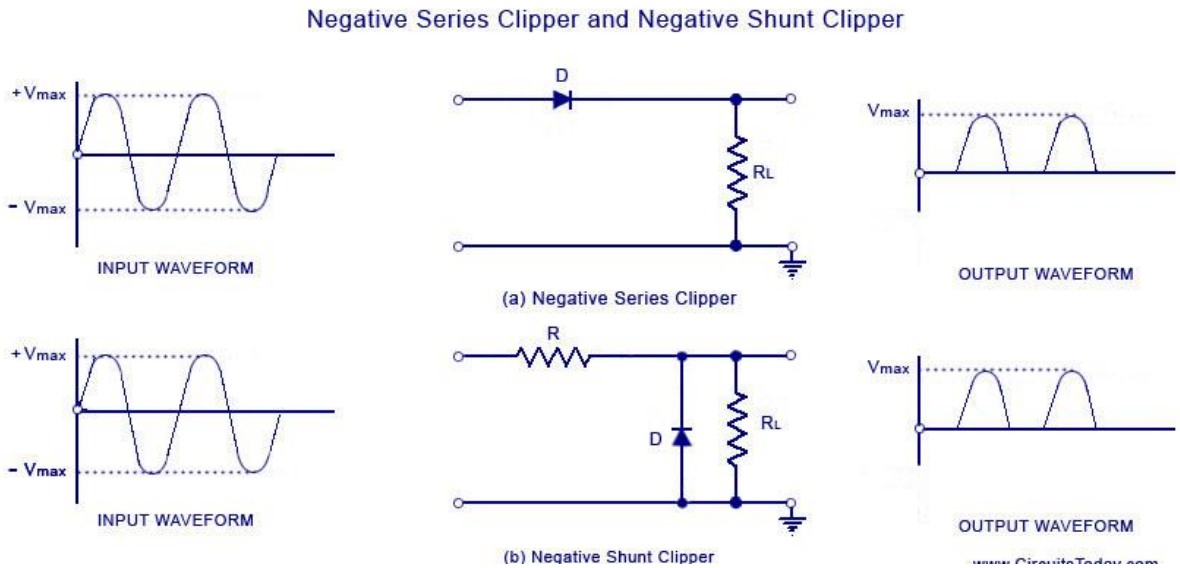

As shown in the figure, the diode is kept in series with the load. During the positive half cycle of the input waveform, the diode 'D' is reverse biased, which maintains the output voltage at 0 Volts. This causes the positive half cycle to be clipped off. During the negative half cycle of the input, the diode is forward biased and so the negative half cycle appears across the output.

In Figure (b), the diode is kept in parallel with the load. This is the diagram of a positive shunt clipper circuit. During the positive half cycle, the diode 'D' is forward biased and the diode acts as a closed switch. This causes the diode to conduct heavily. This causes the voltage drop

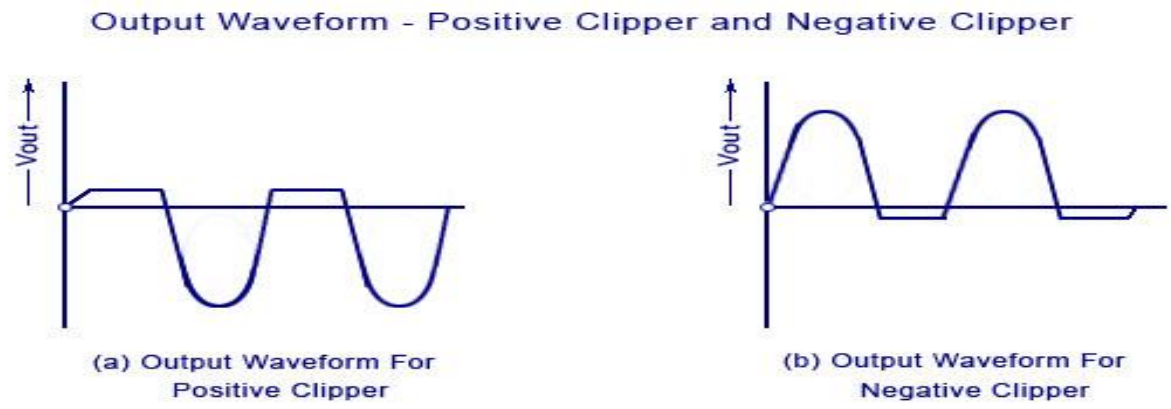
across the diode or across the load resistance $R_L$ to be zero. Thus, output voltage during the positive half cycles is zero, as shown in the output waveform. During the negative half cycles of the input signal voltage, the diode D is reverse biased and behaves as an open switch. Consequently, the entire input voltage appears across the diode or across the load resistance $R_L$ if R is much smaller than $R_L$

***Negative Diode Clipper***

The negative clipping circuit is almost the same as the positive clipping circuit, with only one difference. If the diode in figures (a) and (b) is reconnected with reversed polarity, the circuits will become for a negative series clipper and negative shunt clipper respectively. The negative series and negative shunt clippers are shown in figures (a) and (b) as given below.

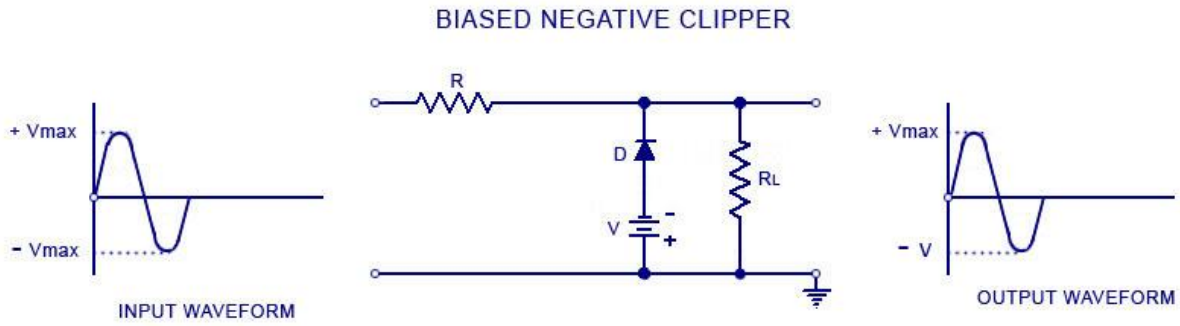



In all the above discussions, the diode is considered to be the ideal one. In a practical diode, the breakdown voltage will exist (0.7 V for silicon and 0.3 V for Germanium). When this is taken into account, the output waveforms for positive and negative clippers will be of the shape shown in the figure below.

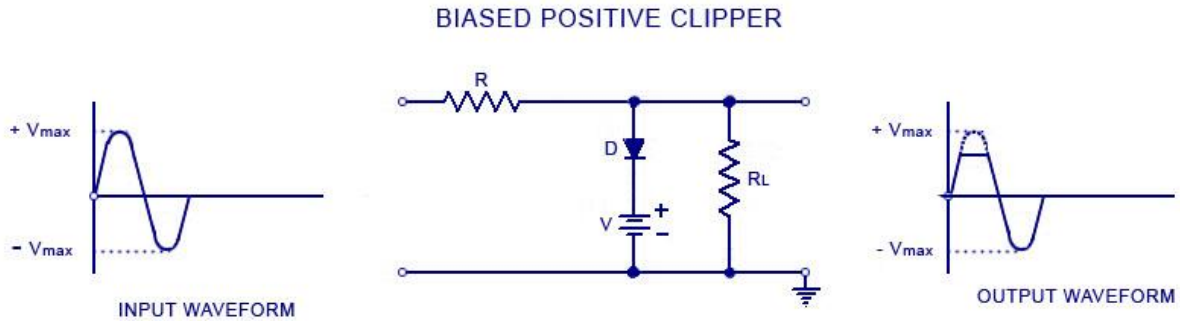


## 2. Biased Positive Clipper and Biased Negative Clipper

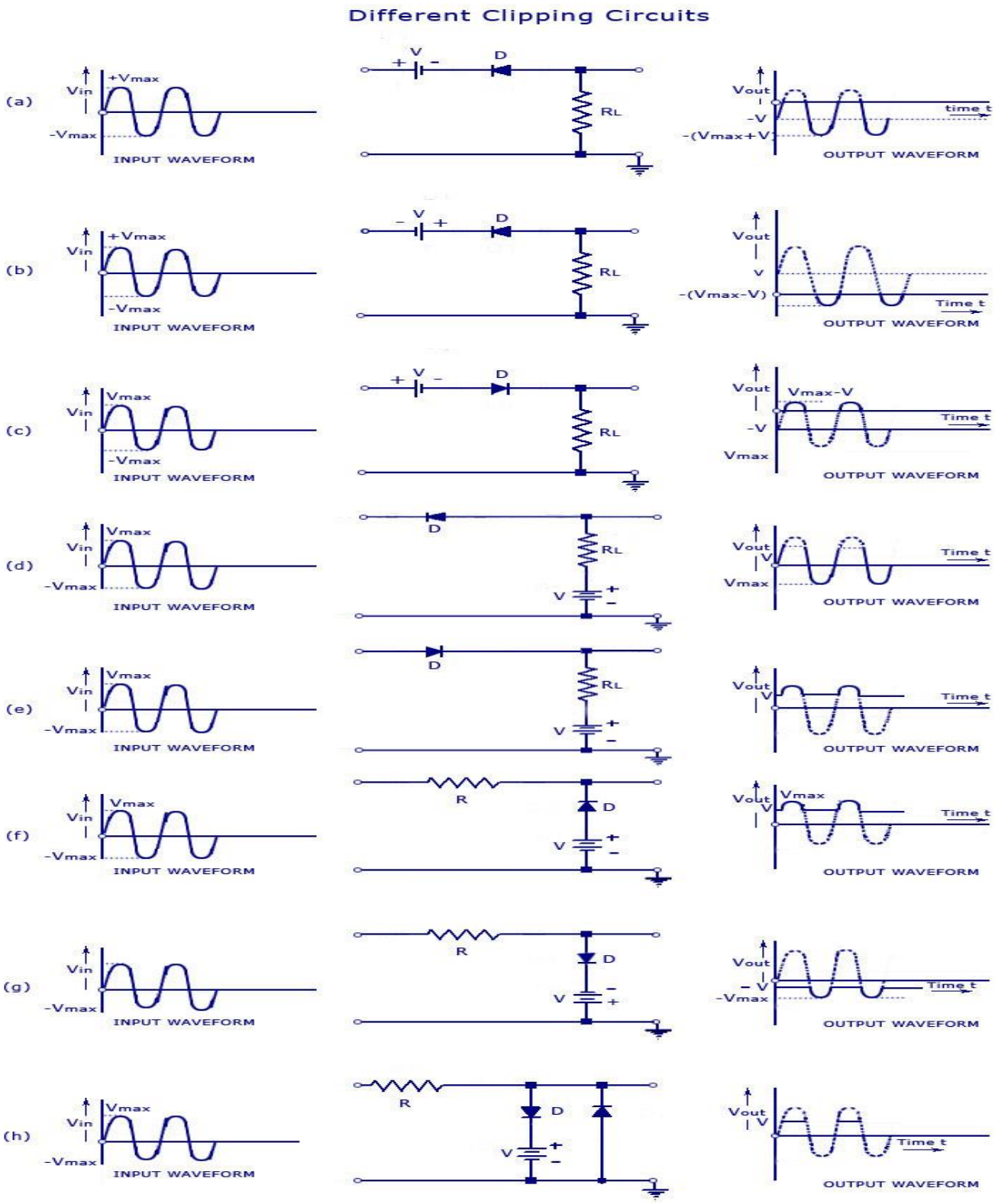
A biased clipper comes in handy when a small portion of positive or negative half cycles of the signal voltage is to be removed. When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper. The circuit diagram and waveform is shown in the figure below.




In a biased clipper, when the input signal voltage is positive, the diode 'D' is reverse-biased. This causes it to act as an open-switch. Thus, the entire positive half cycle appears across the load, as illustrated by output waveform. When the input signal voltage is negative but does not exceed battery the voltage 'V', the diode 'D' remains reverse-biased and most of the input voltage appears across the output. When during the negative half cycle of input signal, the signal voltage becomes more than the battery voltage V, the diode D is forward biased and so conducts heavily. The output voltage is equal to '- V' and stays at '- V' as long as the magnitude of the input signal voltage is greater than the magnitude of the battery voltage, 'V'. Thus, a biased negative clipper removes input voltage when the input signal voltage becomes greater than the battery voltage. Clipping can be changed by reversing the battery and diode connections, as illustrated in figure.

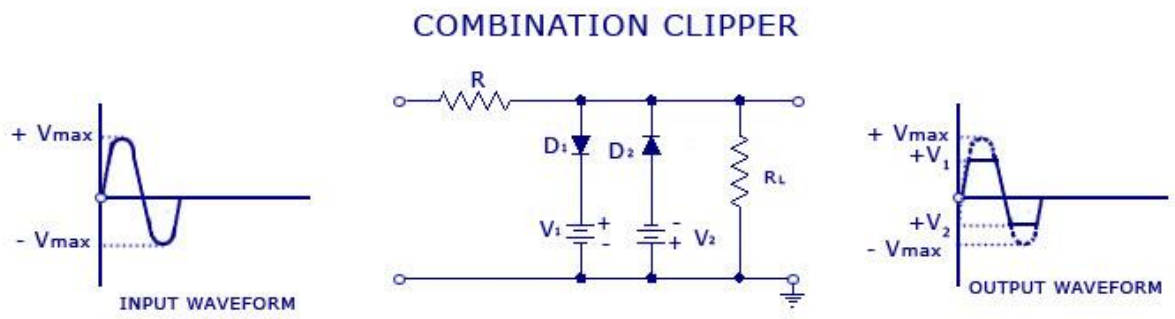


Some of the other biased clipper circuits are given below in the figure. While drawing the wave-shape of the output basic principle discussed above are followed. The diode has been considered as an ideal one.



## 3. Combination Clipper

When a portion of both positive and negative of each half cycle of the input voltage is to be clipped (or removed), combination clipper is employed. The circuit for such a clipper is given in the figure below.




The action of the circuit is summarized below. For positive input voltage signal when input voltage exceeds battery voltage '+ $V_1$'diode $D_1$ conducts heavily while diode '$D_2$'is reversed biased and so voltage '+ $V_1$'appears across the output. This output voltage '+ $V_1$'stays as long as. The input signal voltage exceeds '+ $V_1$'. On the other hand for the negative input voltage signal, the diode '$D_1$' remains reverse biased and diode '$D_2$' conducts heavily only when input voltage exceeds battery voltage '$V_2$' in magnitude. Thus during the negative half cycle the output stays at '- $V_2$'so long as the input signal voltage is greater than '-$V_2$'.

**Drawbacks of Series and Shunt Diode Clippers**

- In series clippers, when the diode is in 'OFF' position, there will be no transmission of the input signal to output. But in the case of high-frequency signals transmission occurs through diode capacitance which is undesirable. This is the drawback of using the diode as a series element in such clippers.
- In shunt clippers, when the diode is in the 'off condition, transmission of input signal should take place to output. But in the case of high-frequency input signals, diode capacitance affects the circuit operation adversely and the signal gets attenuated (that is, it passes through diode capacitance to ground).

**Applications of clipping circuits**

- Used in FM transmitters to reduce noise
- To limit the voltage input to a device
- To modify an existing waveform to the desired output.

# CLAMPER

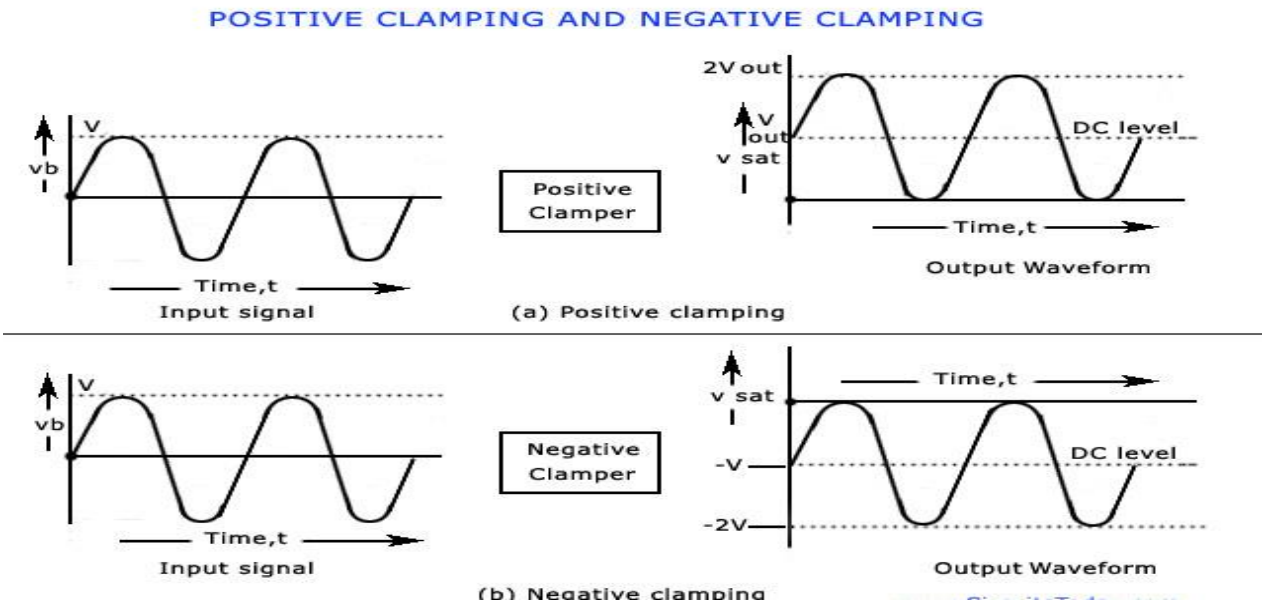
A clamper circuit adds the positive or negative dc component to the input signal so as to push it either on the positive side, as illustrated in figure (a) or on the negative side, as illustrated in figure (b).

*Positive clamper*

The circuit will be called a positive clamper, when the signal is pushed upward by the circuit. When the signal moves upward, as shown in figure (a), the negative peak of the signal coincides with the zero level.

*Negative Clamper*

The circuit will be called a negative clamper, when the signal is pushed downward by the circuit. When the signal is pushed on the negative side, as shown in figure (b), the positive peak of the input signal coincides with the zero level.




**Working of a diode clamping circuit**

For a clamping circuit at least three components â€" a diode, a capacitor and a resistor are required. Sometimes an independent dc supply is also required to cause an additional shift. The important points regarding clamping circuits are:

**(i)** The shape of the waveform will be the same, but its level is shifted either upward or downward,

**(ii)** There will be no change in the peak-to-peak or rms value of the waveform due to the clamping circuit. Thus, the input waveform and output waveform will have the same peak-to-peak value that is, $2V_{max}$. This is shown in the figure above. It must also be noted that same

reading will be obtained in the ac voltmeter for the input voltage and the clamped output voltage.

**(iii)** There will be a change in the peak and average values of the waveform. In the figure shown above, the input waveform has a peak value of $V_{max}$ and average value over a complete cycle is zero. The clamped output varies from 2 $V_{max}$ and 0 (or 0 and -2$V_{max}$). Thus this peak value of the clamped output is 2$V_{max}$ and average value is $V_{max.}$

**(iv)** The values of the resistor R and capacitor C affect the waveform.

**(v)** The values for the resistor R and capacitor C should be determined from the time constant equation of the circuit, t = RC. The values must be large enough to make sure that the voltage across the capacitor C does not change significantly during the time interval the diode is non-conducting. In a good clamper circuit, the circuit time constant t = RC should be at least ten times the time period of the input signal voltage.

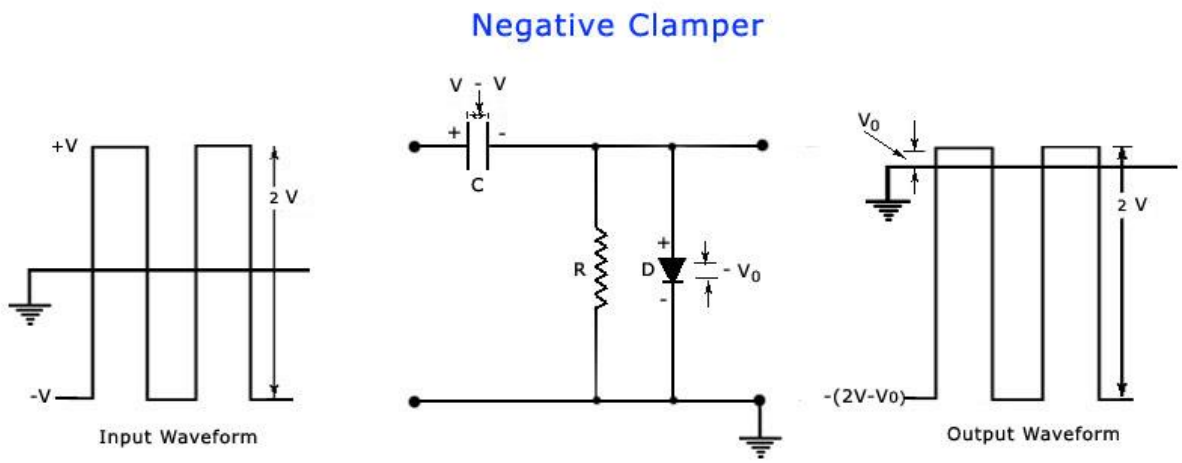
It is advantageous to first consider the condition under which the diode becomes forward biased.

Clamping circuits are often used in television receivers as dc restorers. The signal that is sent to the TV receiver may lose the dc components after being passed through capacitive coupled amplifiers. Thus, the signal loses its black and white reference levels and the blanking level. Before passing these signals to the picture tube, these reference levels have to be restored. This is done by using clamper circuits. They also find applications in storage counters, analog frequency meter, capacitance meter, divider and stair-case waveform generator.

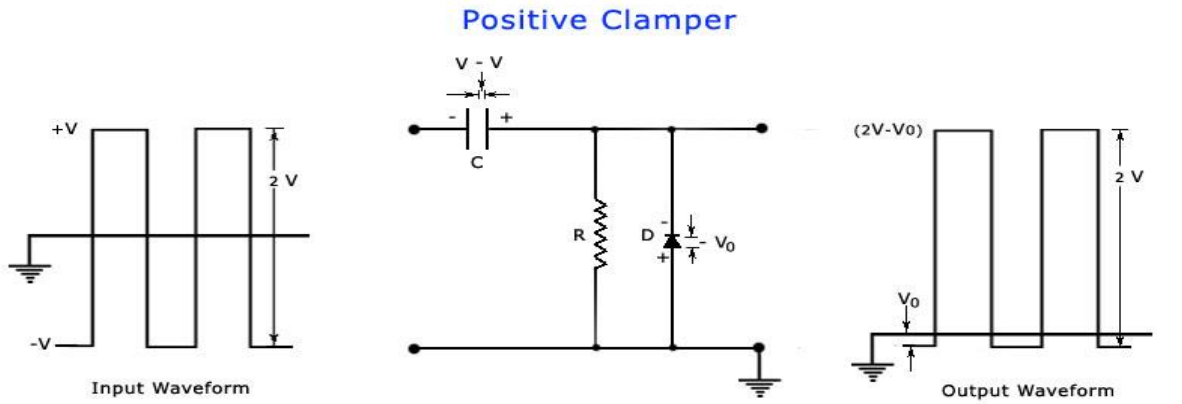
Consider a negative clamping circuit, a circuit that shifts the original signal in a vertically downward direction, as shown in the figure below. The diode D will be forward biased and the capacitor C is charged with the polarity shown, when an input signal is applied. During the positive half cycle of input, the output voltage will be equal to the barrie r potential of the diode, $V_0$ and the capacitor is charged to ($V - V_Q$). During the negative half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus, there will be no effect on the capacitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input waveform. Thus, during negative input, the output voltage will be the sum of the input voltage and the capacitor voltage and is equal to – V – (V â€" $V_0$) or – (2 V – $V_0$). The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to $V_0$-[-(2V-$V_0$)] Â Â or Â 2 V.

The figure shown below can be modified into a positive clamping circuit by reconnecting the diode with reversed polarity. The positive clamping circuit moves the original signal in a vertically upward direction. A positive clamping circuit is shown in the figure below. It contains a diode D and a capacitor C as are contained in a negative clamper. The only difference in the circuit is that the polarity of the diode is reversed. The remaining explanation regarding the working of the circuit is the same as it is explained for the negative clamper.

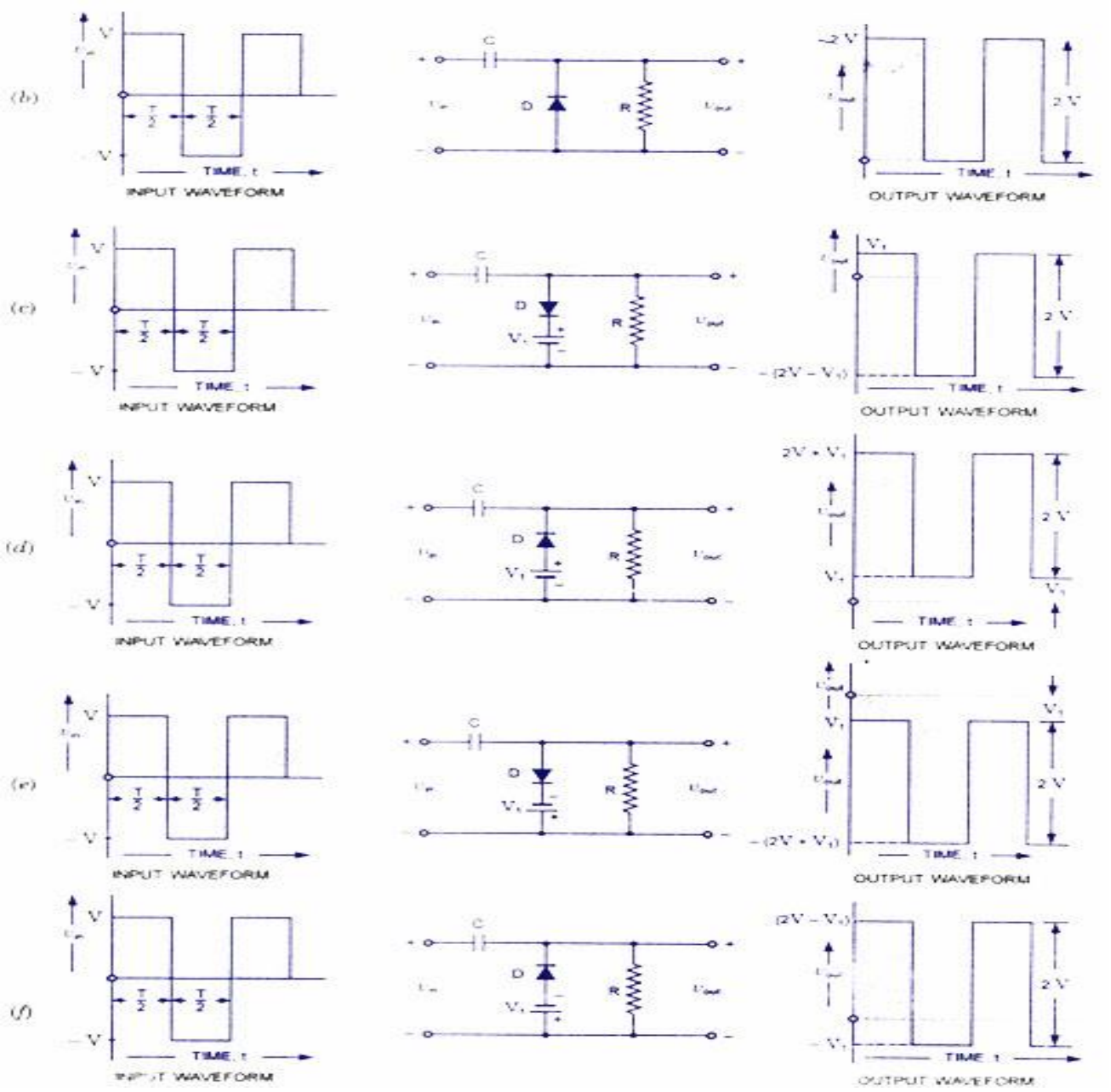
To remember which way the dc level of a signal moves, look at the figure shown below. Notice that the diode arrows point downward, the same direction as the dc shift.




Similarly, in the figure shown below, the diode arrow points upward, again the same direction as the dc shifts. It means that when the diode points upward. We have a positive dc clamper and when the diode points downward, the circuit is a negative dc clamper.




A number of clamping circuits with their effect on the input signal are shown in the figure given below. All the figures shown below have the input and output signals in square waves, the same procedure can be used for sinusoidal inputs. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal wave signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response, as illustrated in figure (g) for a network appearing in figure (f). The diodes have been assumed to be ideal and 5 RC Â» T/2 in drawing the output waveforms.




**Applications of clamping circuits**

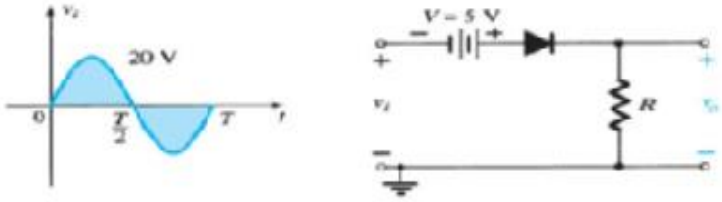
- They find some applications in sonar and radar testing
- Used as voltage doublers
- They are used to remove distortions in a circuit
- Used in video processing equipment like TV

**EXAMPLE** Determine the output waveform for the sinusoidal input of Fig.

***Solution:***

**Step 1:** The output is again directly across the resistor $R$.

**Step 2:** The positive region of $v_i$ and the dc supply are both applying "pressure" to turn the diode on. The result is that we can safely assume the diode is in the "on" state for the entire range of positive voltages for $v_i$. Once the supply goes negative, it would have to exceed the dc supply voltage of 5 V before it could turn the diode off.



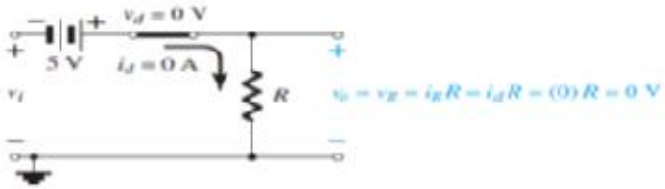

*Series clipper for Example*

**Step 3:** The transition model is substituted in Fig. and we find that the transition from one state to the other will occur when

$$v_i + 5\text{ V} = 0\text{ V}$$

or

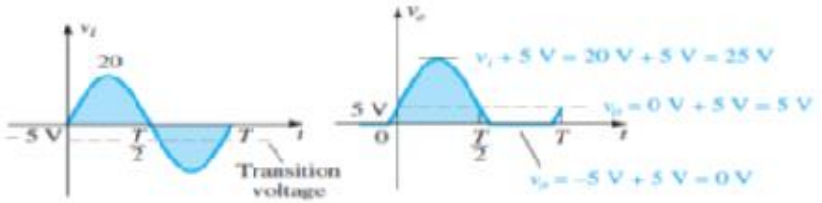
$$v_i = -5\text{ V}$$




*Determining the transition level for the clipper of Fig.*

**Step 4:** In Fig. a horizontal line is drawn through the applied voltage at the transition level. For voltages less than −5 V the diode is in the open-circuit state and the output is 0 V, as shown in the sketch of $v_o$. Using Fig. , we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

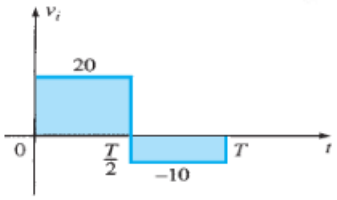
$$v_o = v_i + 5\text{ V}$$



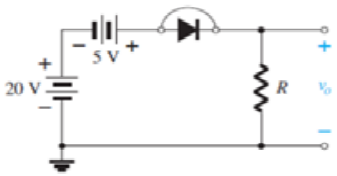

The analysis of clipper networks with square-wave inputs is actually easier than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting $v_o$ plotted in the proper time frame. The next example demonstrates the procedure.

**EXAMPLE** Find the output voltage for the network examined in above example, if the applied signal is the square wave

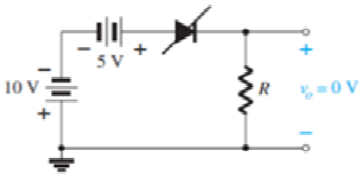
***Solution:*** For $v_i = 20\ \text{V}\ (0 \rightarrow T/2)$ the network of Fig. 2.78 results. The diode is in the short-circuit state, and $v_o = 20\ \text{V} + 5\ \text{V} = 25\ \text{V}$. For $v_i = -10\ \text{V}$ the network



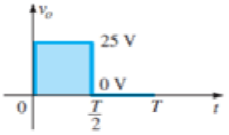

results, placing the diode in the "off" state, and $v_o = i_R R = (0)R = 0\ \text{V}$. The resulting output voltage appears in Fig. 2.80.




$v_o$ at $v_i = +20$ V.




$v_o$ at $v_i = -10$ V.

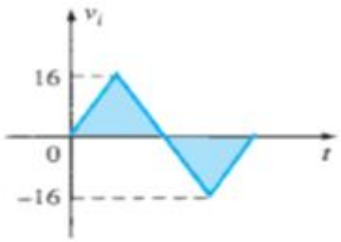


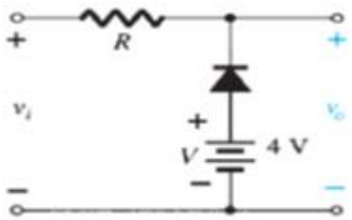

*Sketching $v_o$ for Example 2.19.*

**EXAMPLE** Determine $v_o$ for the network

***Solution:***

**Step 1:** In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor $R$.



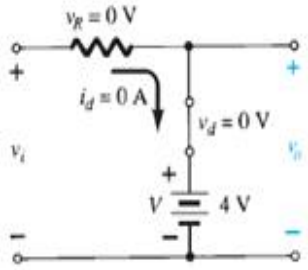



**Step 2:** The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is on the output will be 4 V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$ whenever the diode is off.

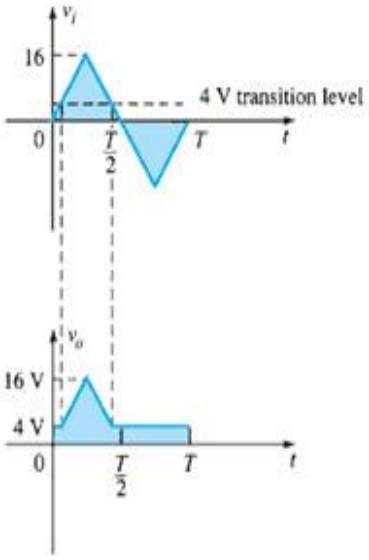
**Step 3:** The transition level of the input voltage can be found from Fig. . by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition. The result is a change in state when

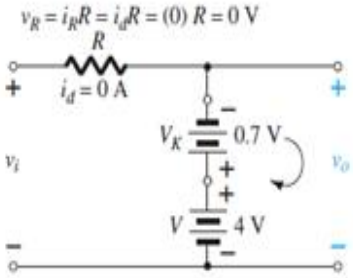
$$v_i = 4\text{ V}$$

**Step 4:** In Fig. .he transition level is drawn along with $v_o = 4$ V when the diode is on. For $v_i \geq 4$ V, $v_o = 4$ V, and the waveform is simply repeated on the output plot.




*Determining the transition level*




*Determining the transition level for the network*

To examine the effects of the knee voltage $V_K$ of a silicon diode on the output response, the next example will specify a silicon diode rather than the ideal diode equivalent.

# MODULE – 2

## Transistor

A Transistor is a three terminal semiconductor device that regulates current or voltage flow and acts as a switch or gate for signals.

**Constructional Details**

- The transistor is a three terminal semiconductor device which is formed by connecting two diodes back to back. Hence it has got two PN junctions. Three terminals are drawn out of the three semiconductor materials present in it.
- Two types of transistors, namely, PNP and NPN which means an N-type material between two P-types, and the other is a P-type material between two N-types, respectively.

The three terminals of a transistor is denoted as Emitter, Base and Collector terminals. The abbreviation BJT, from bipolar junction transistor, is often applied to this three-terminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material.

A detailed functionality of each of the terminals is discussed below.

**Emitter**

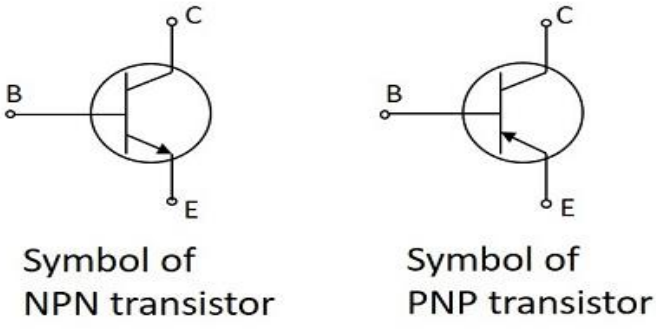
- Emitter has a moderate size and is heavily doped as its main function is to supply a number of majority carriers, i.e. either electrons or holes.
- As this emits majority charge carriers, it is called as an Emitter denoted as 'E'.

**Base**

- Base terminal (denoted as 'B') is thin and lightly doped.
- Its main function is to pass the majority carriers from the emitter to the collector.

**Collector**

- The name collector (denoted as 'C') implies its function of collecting the majority carriers emitted from the Emitter side.
- It is a bit larger in size than emitter and base. It is moderately doped.




**(a)** **(b)**

**Figure 1: Symbols for a) NPN Transistor; b) PNP Transistor**

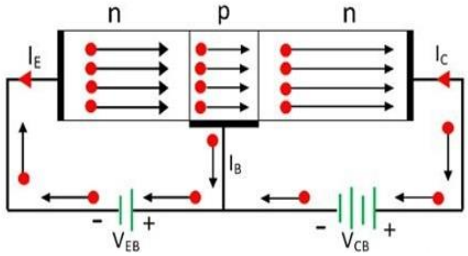
The arrow-head in the above figures indicated the emitter of a transistor. As the collector of a transistor has to dissipate much greater power, it is made large. Due to the specific functions of emitter and collector, they are not interchangeable.

## Bipolar Junction Transistor

BJT is a three terminal bidirectional electronic device. The terminals are collector base and emitter. It has two junctions. A layer of one type crystal is sandwiched by other two layers of same type. Therefore, there are two types of transistors i.e. NPN transistor and PNP transistor.

### NPN Transistor

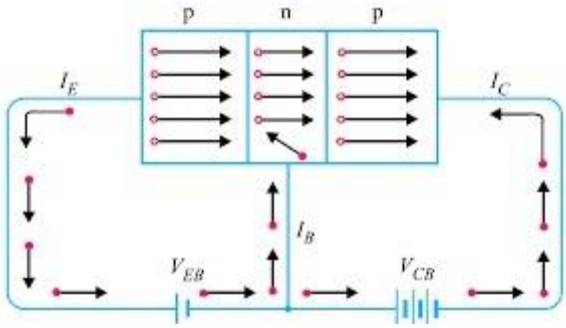
The transistor in which one p-type material is placed between two n-type materials is known as **NPN transistor**. In NPN transistor, the direction of **movement of an electron** is from the **emitter to collector** region due to which the current constitutes in the transistor.
The circuit diagram of the NPN transistor is shown in the figure below. The forward biased is applied across the emitter-base junction, and the reversed biased is applied across the collector-base junction. The forward biased voltage $V_{EB}$ is small as compared to the reverse bias voltage $V_{CB}$.




The emitter of the NPN transistor is heavily doped. When the forward bias is applied across the emitter, the majority charge carriers move towards the base. This causes the emitter current $I_E$. The electrons enter into the P-type material and combine with the holes.
The base of the NPN transistor is lightly doped. Due to which only a few electrons are combined and remaining constitutes the base current $I_B$. This base current enters into the collector region.
The reversed bias potential of the collector region applies the high attractive force on the electrons reaching collector junction. Thus attract or collect the electrons at the collector. The whole of the emitter current is entered into the base. Thus, we can say that the emitter current is the sum of the collector or the base current i.e. $I_E = I_C + I_B$.

### PNP Transistor

The transistor in which one n-type material is placed between two p-type materials is known as **PNP transistor.** In PNP transistor, the direction of **movement of a hole** is from the **emitter to collector** region due to which the current constitutes in the transistor.




The circuit diagram of the PNP transistor is shown here. The forward biased is applied across the emitter-base junction, and the reversed biased is applied across the collector-base junction. The forward biased voltage $V_{EB}$ is small as compared to the reverse bias voltage $V_{CB}$. The emitter of the NPN transistor is heavily doped. When the forward bias is applied across the emitter, the majority charge carriers i.e. the holes move towards the base. This causes the emitter current $I_E$. The holes enter into the N-type material and combine with the electrons.

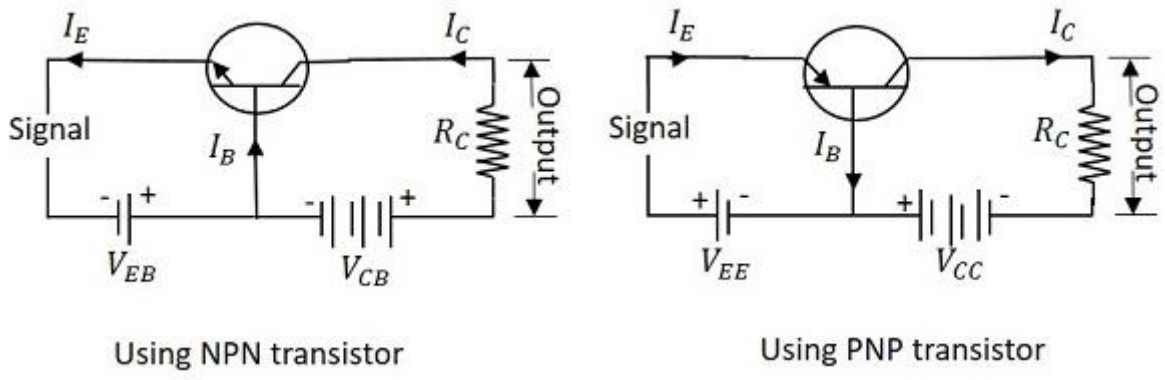
The base of the PNP transistor is lightly doped. Due to which only a few holes are combined and remaining constitutes the base current $I_B$. This base current enters into the collector region. The reversed bias potential of the collector region applies the high attractive force on the electrons reaching collector junction. Thus attract or collect the holes at the collector. The whole of the emitter current is entered into the base. Thus, we can say that the emitter current is the sum of the collector and the base current i.e. $I_E = I_C + I_B$.

**TRANSISTOR CONFIGURATIONS:**

Based on the three terminals of the transistor, three different configurations are possible :

1) Common Base – Base Terminal common to both emitter and collector terminal.
2) Common Emitter – Emitter terminal is common to both base and collector terminal.
3) Common Collector – Collector terminal is common to both emitter and base terminal.

**COMMON BASE CONFIGURATION:**




**(a)** **(b)**

**Figure 2: CB Configuration for a) NPN Transistor; b) PNP Transistor**

The operation of CB configuration using NPN transistor is described below.

- **No Bias Condition** – Both input side (Emitter-Base) and output side (Base-Collector) is not provided with external potential. Here, depletion layer is formed in both the input and output junctions due to concentration difference at the junctions.
- Next the input and output is made forward and reversed biased, respectively, as shown in the above figure. Since, the negative terminal is connected to n-type **(Figure 2 (a)),** the electrons from the emitter side is repelled towards the collector through the base. In this process, some amount of electrons get recombined with the holes present as the majority charge carriers in the base (p-type). This results in a current in the emitter side denoted as $I_E$. These charge carriers are collected across the collector terminal and results in a current denoted as $I_C$.

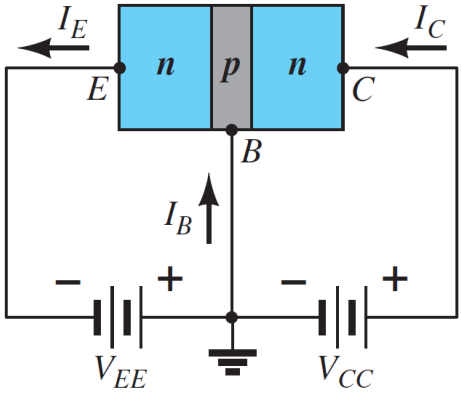



**Figure 3: Under Forward and Reverse Bias Condition**

The magnitude of the base current is typically on the order of microamperes, as compared to milli-amperes for the emitter and collector currents. Applying Kirchhoff's current law to the transistor, we can obtain

$$I_E = I_B + I_C$$

The collector current, however, comprises two components—the majority and minority carriers

**Current amplification factor:**

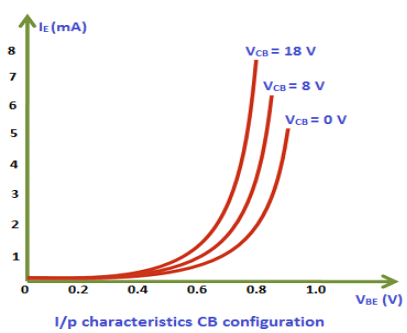
At constant $V_{CB}$ , it is the ratio between change in collector current to change in emitter current.

i.e. $\alpha = \frac{\Delta I_C}{\Delta I_E}$ at constant $V_{CB}$ for variable current or AC current.

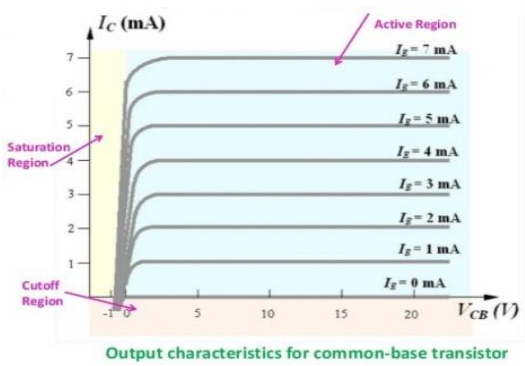
$\alpha = \frac{I_C}{I_E}$ at constant $V_{CB}$ for fixed current or DC current.

$\alpha$ =0.9 to 0.99

$\alpha < 1$




I/p characteristics CB configuration




Output characteristics for common-base transistor

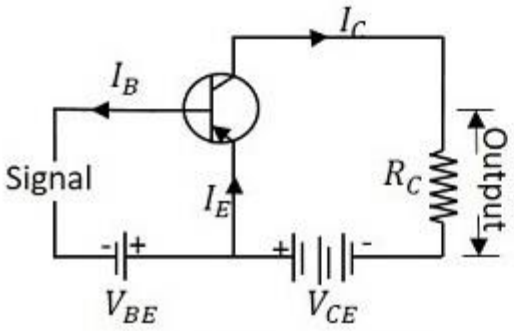
**Expression for collector current:** $I_C = \alpha I_E + I_{CBO}$

**Concept of $I_{CBO}$ :**

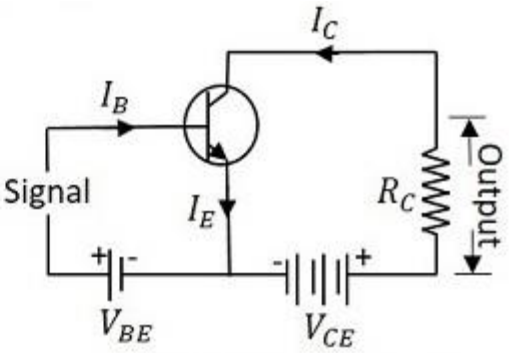
When emitter is open, $I_B = 0$ ,there is very small current in collector base circuit in the form of some μA. This is known as $I_{CBO}$(collector-base current with open emitter) or leakage current. This is caused by minority charge carriers. $I_{CBO}$ is constant for the entire circuit operation whatever the change in input.

## Common Emitter Configuration

In common base configuration the emitter is common to both input and output circuit and this common terminal is grounded.



Using PNP transistor



Using NPN transistor

**Current amplification factor:**

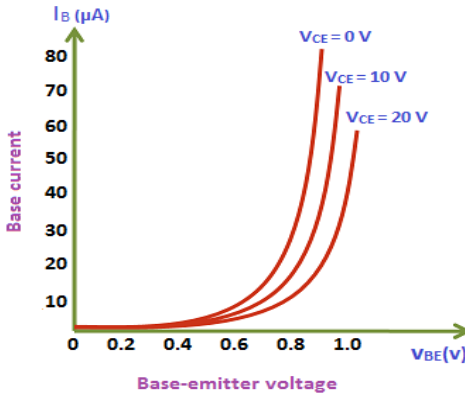
At constant $V_{CE}$ , it is the ratio between change in collector current to change in base current.

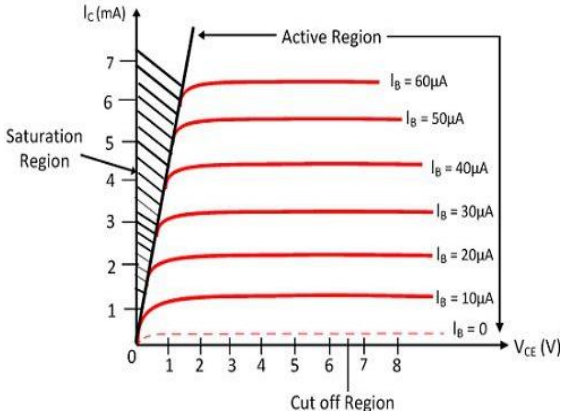
i.e. β= $\frac{\Delta I_C}{\Delta I_B}$ at constant $V_{CE}$ for variable current or AC current.

β= $\frac{I_C}{I_B}$ at constant $V_{CE}$ for fixed current or DC current.

20 < β < 500

$I_C = \beta * I_B$



**Relation between $\alpha$ and β:**

$$I_E = I_C + I_B$$

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\boldsymbol{\alpha = \frac{\beta}{1+\beta}} \text{ and } \boldsymbol{\beta = \frac{\alpha}{1-\alpha}}$$

**Expression for output current:**

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$(1-\alpha)I_C = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

$$\boldsymbol{I_C = \beta I_B + I_{CEO}}$$

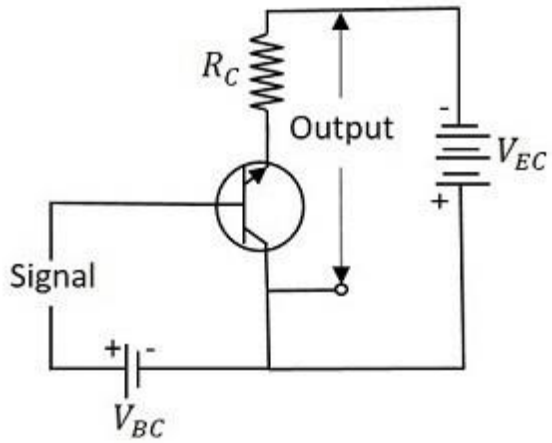
**So,** $\boldsymbol{I_{CEO} = \frac{I_{CBO}}{1-\alpha}}$

**Concept of $I_{CEO}$ :**

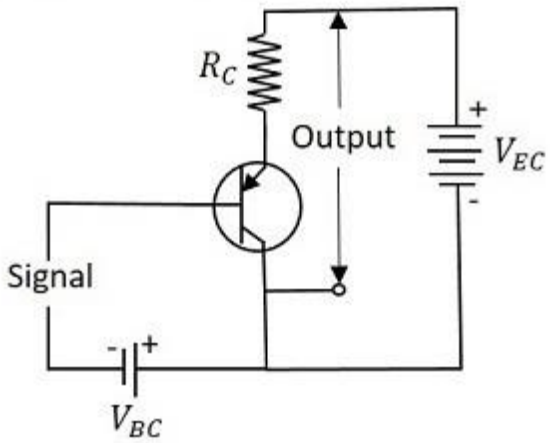
When base is open, $I_B = 0$ ,a small leakage current known as $I_{CEO}$(collector-emitter current with open base) flows in output circuit.

**<u>Common Collector Configuration</u>**

In common collector configuration the collector is common to both input and output circuit and this common terminal is grounded.




Using NPN transstor




Using PNP transistor

**Current amplification factor:**

At constant $V_{CE}$ , it is the ratio between change in collector current to change in emitter current.

i.e. $\gamma = \frac{\Delta I_E}{\Delta I_B}$ at constant $V_{CE}$ for variable current or AC current.

$\gamma = \frac{I_E}{I_B}$ at constant $V_{CE}$ for fixed current or DC current.

**Relation between $\alpha$, $\beta$ and γ:**

$$I_E = I_C + I_B$$

$$\gamma I_B = I_B + \beta I_B$$

$$\boldsymbol{\gamma = 1 + \beta}$$

$$\boldsymbol{\beta = \gamma - 1}$$

$$\gamma = 1 + \beta$$

$$\gamma = 1 + \frac{\alpha}{1 - \alpha}$$

$$\boldsymbol{\gamma = \frac{1}{1 - \alpha}}$$

**Expression for output current:**

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_C + I_B$$

$$I_E = \alpha I_E + I_{CBO} + I_B$$

$$(1 - \alpha) I_E = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha}$$

$$\boldsymbol{I_E = \gamma I_B + I_{CEO}}$$

## TRANSISTOR BIASING:

- To operate the transistor in the desired region and to obtain faithful amplification, we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is known as **biasing of the transistor**.
- Since DC voltages are used to bias the transistor, it is called as **DC biasing**.

**NEED FOR BIASING:**

- To operate the transistor in the desired region by maintaining the proper operating point thereby achieving faithful amplification.

**Faithful amplification:**

- The process of raising the strength of a weak signal without any change in its general shape is known as a **faithful amplification.** It is the process of obtaining complete

portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input.

- The key factor to achieve the faithful amplification is that the base emitter junction of transistor must be forward biased and collector junction must be reverse biased.

**To ensure this, the following conditions must be specified.**

1. **Proper Zero Signal Collector Current**:

   - The value of zero signal collector current should be at least equal to the maximum collector current due to signal alone.

2. **Proper Minimum Base-emitter Voltage**:

   - In order to achieve faithful amplification, the base emitter voltage $V_{BE}$ should not fall below 0.5 V for germanium transistor and 0.7 V for silicon transistor. If the base-emitter voltage VBE is greater than this voltage, the potential barrier is overcome and hence the base current and collector currents increase sharply.

3. **Proper Minimum Collector Emitter Voltage**:

   - For faithful amplification, the collector emitter voltage $V_{CE}$ should not fall below 0.5 V for germanium and 1.0 V for silicon transistors. This is called **Knee Voltage**. If VCE is lesser than the knee voltage, the collector base junction will not be properly reverse biased. Then the collector cannot attract the electrons which are emitted by the emitter and they will flow towards base which increases the base current. Thus the value of β falls.

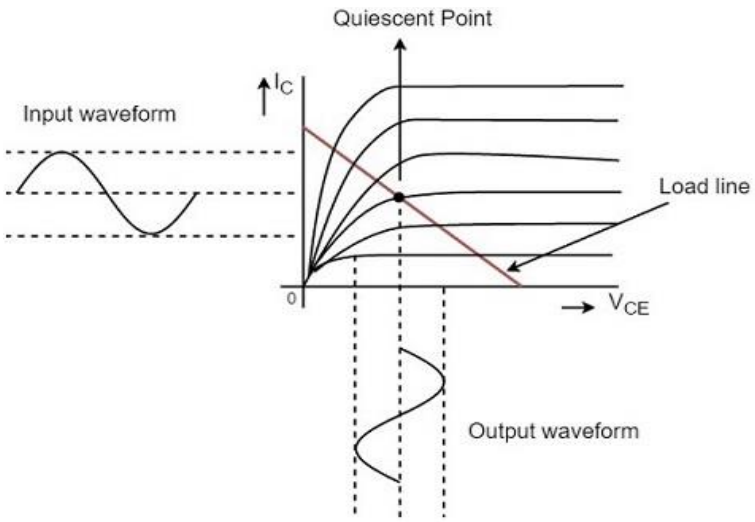



**Figure 1: Faithful Amplification**

**DC LOAD LINE:**

- The line joining the maximum value of collector current and collector-emitter voltage in Y-axis and X-axis, respectively, is called as **Load line.**

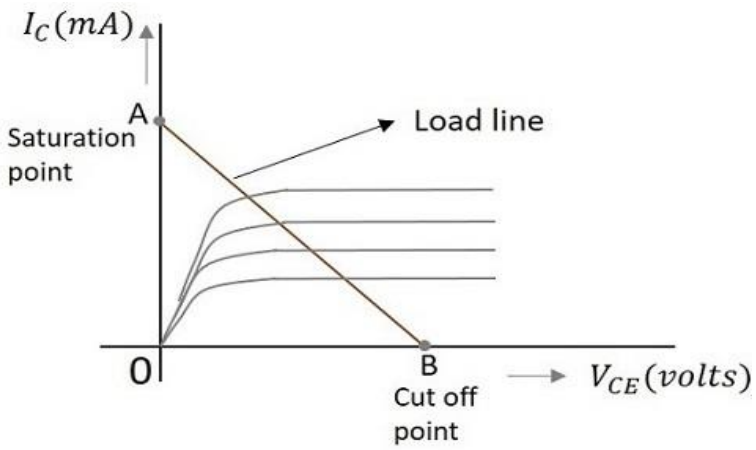



**Figure 2: Load Line**

- The region that lies between these two is the **linear region**.
- **A transistor acts as a good amplifier in this linear region.**
- If this load line is drawn only when DC biasing is given to the transistor, but no input signal is applied, then such a load line is called as a **DC load line**. Whereas the load line drawn under the conditions when an input signal along with the DC voltages are applied, such a line is called as an **AC load line**.

**DC OPERATING POINT (OR) QUIESCENT POINT:**

- The DC voltages (bias) applied establishes a fixed level of current and voltage to determine an operating point on the output characteristics graph. This defines the region that will be employed for amplification of the applied input signal. Since the operating point is a fixed point on the characteristics, it is called as the **Quiescent point (Q - Point).**
- The operating point should not get disturbed as it should remain stable to achieve faithful amplification. Hence the quiescent point or Q-point is the value where the faithful amplification is achieved.
- The operating point must be chosen such that it lies in the active region and it helps in the reproduction of complete signal without any loss.

**If the operating point is considered near to the saturation point, then the amplified output signal is shown below.**

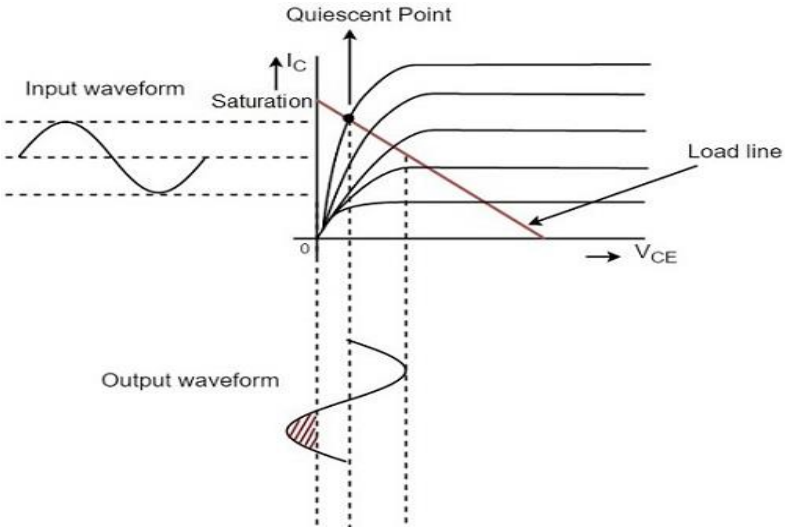



**Figure 3: Operating point near to saturation region**

**If the operation point is considered near to the cut-off point, then the amplified output signal is shown below.**

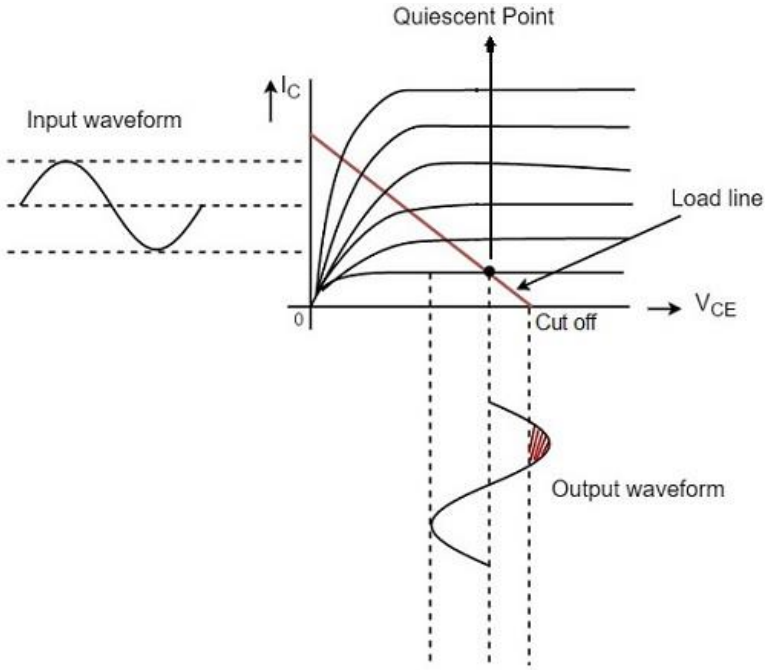



**Figure 4: Operating point near to cut-off region**

**Note**: From Figures 2, 3, and 4, it can be noticed that the selection of operating point is a crucial factor to achieve faithful amplification.

**TYPES OF BIASING CIRCUIT:**

There are different types of biasing circuits:

- **Fixed-bias circuit**

- Emitter-stabilized bias circuit
- **Voltage divider bias circuit**
- DC bias with voltage feedback

**FIXED BIAS CIRCUIT:**

- In this method, a resistor RB is connected in base, as the name implies. The required zero signal base current is provided by $V_{CC}$ which flows through $R_B$. The base emitter junction is forward biased, as base is positive with respect to emitter.

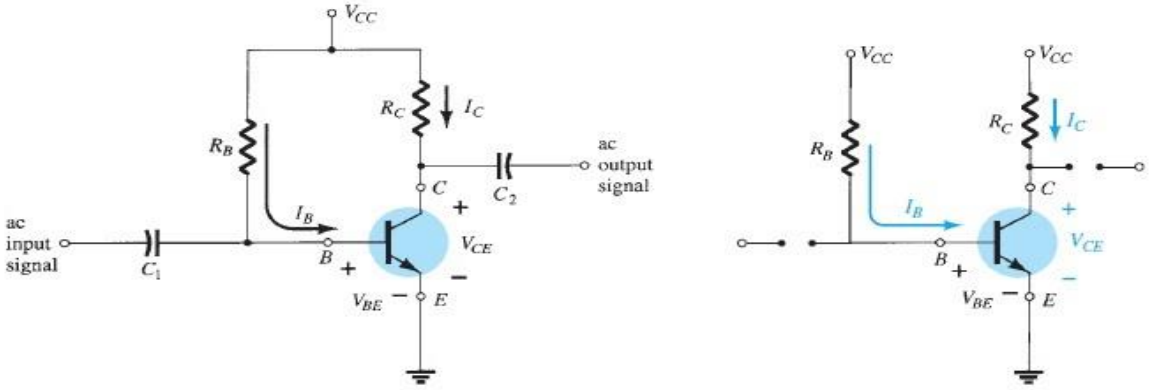



**Figure 5: Fixed bias configuration**

**Analysis of the configuration**

- Locate 2 main loops:
  - BE loop (input loop)
  - CE loop(output loop)

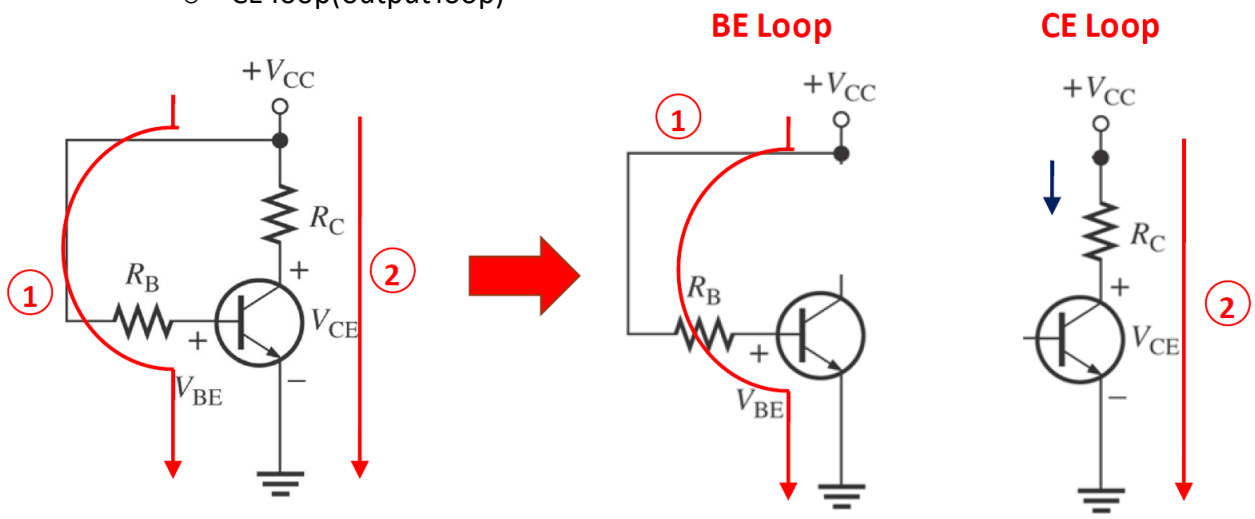



**Figure 6: Fixed bias configuration - I**

**BE Loop Analysis:**

From KVL

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad (1)$$

From **Equation 1**, we can obtain

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad (2)$$

**CE Loop Analysis:**

From KVL

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad (3)$$

From **Equation 3**, we can obtain

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \quad (4)$$

**Transistor Saturation**

For a transistor operating in the saturation region, the current is a maximum value for the particular design. Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted. During saturation the current is relatively high and the voltage $V_{CE}$ is assumed to be zero volts. Applying Ohm's law, the resistance between collector and emitter terminals can be determined as follows:

$$V_{CE(sat)} = V_{CC} - I_{C(sat)} R_C = 0$$

$$\mathbf{I_{C(sat)} = \frac{V_{CC}}{R_C}}$$

**Load-Line Analysis**

The output equation that relates the variables $I_C$ and $V_{CE}$ in the following manner:

$$V_{CE} = V_{CC} - I_C R_C$$

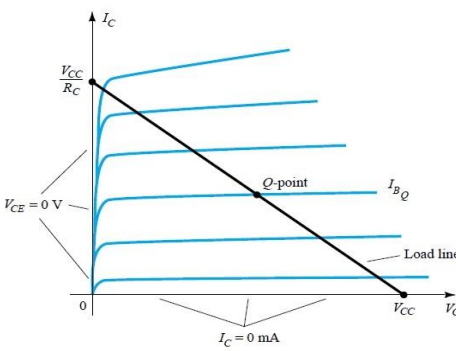
The output characteristics of the transistor also relate the same two variables $I_C$ and $V_{CE}$. In essence, therefore, we have a network equation and a set of characteristics that employ the same variables. The common solution of the two occurs where the constraints established by each are satisfied simultaneously. In other words, this is similar to finding the solution of two simultaneous equations: one established by the network and the other by the device characteristics.

If we *choose* IC to be 0 mA, we are specifying the horizontal axis as the line on which one point is located, we find that

$$V_{CE} = V_{CC} - (0) R_C$$

$$\mathbf{V_{CE} = V_{CC}}$$

During saturation the current is relatively high and



the voltage *VCE* is assumed to be zero volts.

$V_{CE(sat)} = V_{CC} - I_{C(sat)}R_C = 0$

$$\mathbf{I_{C(sat)}} = \frac{V_{CC}}{R_C}$$

The load line is drawn on the output characteristic by joining the two points which signifies the cut-off and saturation condition.

**Advantages**

- The circuit is simple.
- Only one resistor RE is required.
- Biasing conditions are set easily.
- No loading effect as no resistor is present at base-emitter junction.

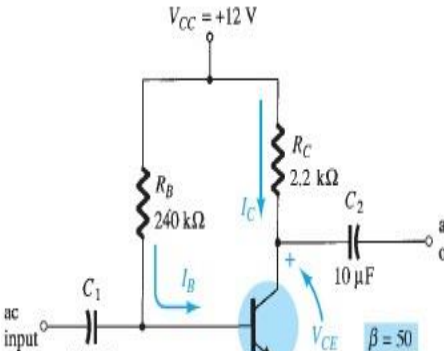
**Disadvantages**

- The stability factor is very high. So, there are strong chances of thermal run away.
- Hence, this method is rarely employed

**Example 1:**

Determine the dc bias voltage $V_{CE}$ and the current $I_C$ for the fixed bias circuit with $V_{CC}$=12V, $R_B$ =240K, $R_C$ =2.2K, β=50.

Also find $I_B$ , $V_C$ , $V_B$ , $V_{BC}$ ?




**ans**:-

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{12 - 0.7}{240K}$$

$$\mathbf{I_{BQ} = 47.08\mu A}$$

$I_C = \beta I_B$

$I_C = 50 * 47.08\mu A$

$$\mathbf{I_{CQ} = 2.35mA}$$

$V_{CE} = V_{CC} - I_C R_C$

$V_{CE} = 12 - (2.35mA * 2.2K)$

$\mathbf{V_{CE}}$ **=6.83V**

$V_B = V_{BE}$

$$\mathbf{V_B = 0.7V}$$

$V_C = V_{CE}$

$\mathbf{V_C = 6.83V}$

$V_{BC} = V_B - V_C$

$V_{BC} = 0.7 - 6.83$

$\mathbf{V_{BC} = -6.83V}$

## VOLTAGE- DIVIDER BIAS CIRCUIT:

- The voltage divider bias method is the most stable biasing circuit. Here, two resistors $R_1$ and $R_2$ are employed, which are connected to $V_{CC}$ in the input side of the circuit. The resistor $R_E$ is used in the emitter to provide stabilization.
- The name of this biasing configuration comes from the fact that the two resistors $R_1$ and $R_2$ form a voltage or potential divider network across the supply with their center point junction connected the transistors base terminal as shown.

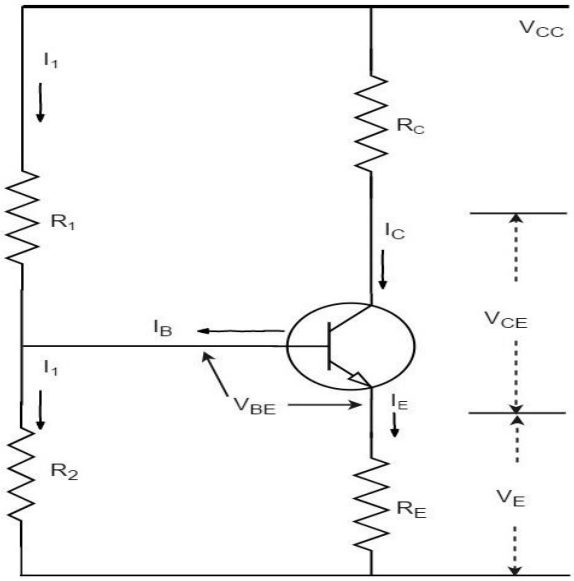



**Figure 7: Voltage divider bias configuration**

**Analysis of the configuration**

1. **Input Side (To find $I_B$):**

Here, we first simplify the input side of the circuit as discussed below.

a) To find the Thevenin's equivalent voltage
b) To find the Thevenin's equivalent resistance.

To determine the aforementioned, the input side of Figure 7 can be redrawn as shown below

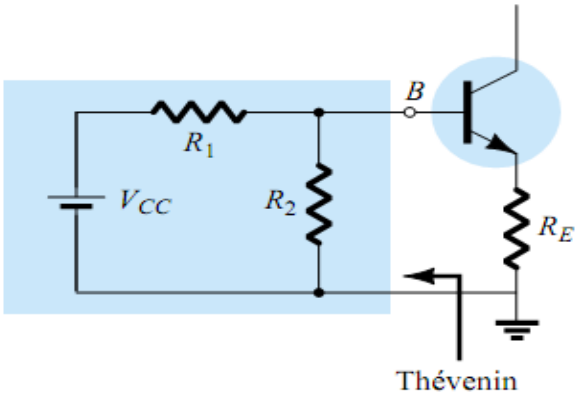



**Figure 8: Alternate input configuration**

**Thevenin's equivalent voltage:**

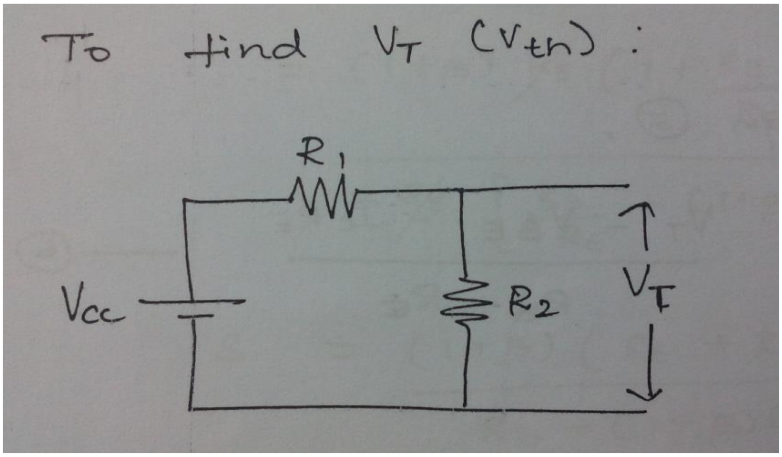



**Figure 9: Determination of $V_{th}$ / $V_T$ / $V_B$**

By Voltage division rule

$$\boldsymbol{V_{TH} = \frac{V_{CC} * R_2}{(R_1 + R_2)}}$$

**Thevenin's equivalent resistance:**

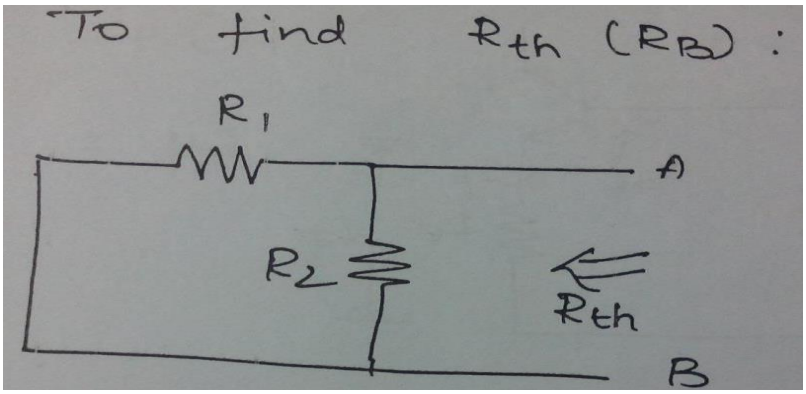



**Figure 10: Determination of $R_{TH}$**

The equivalent resistance is given by

$$R_{TH} = \frac{R_1 R_2}{(R_1 + R_2)}$$

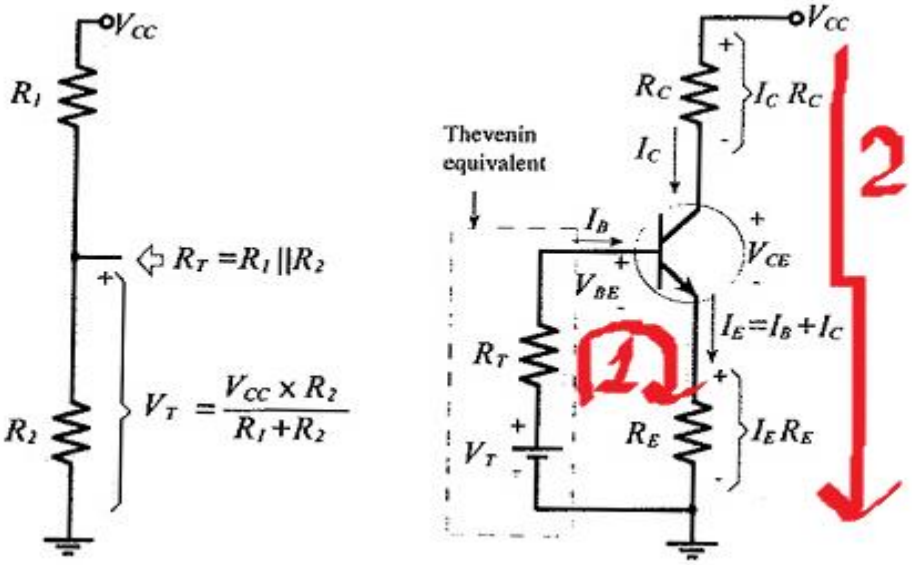



**Figure 11: Equivalent diagram**

**Applying KVL in Loop 1:**

$$V_T - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$V_T - I_B R_{TH} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\boxed{I_B = \frac{V_T - V_{BE}}{(R_{TH} + (\beta + 1) R_E)}}$$

**Applying KVL in Loop 2:**

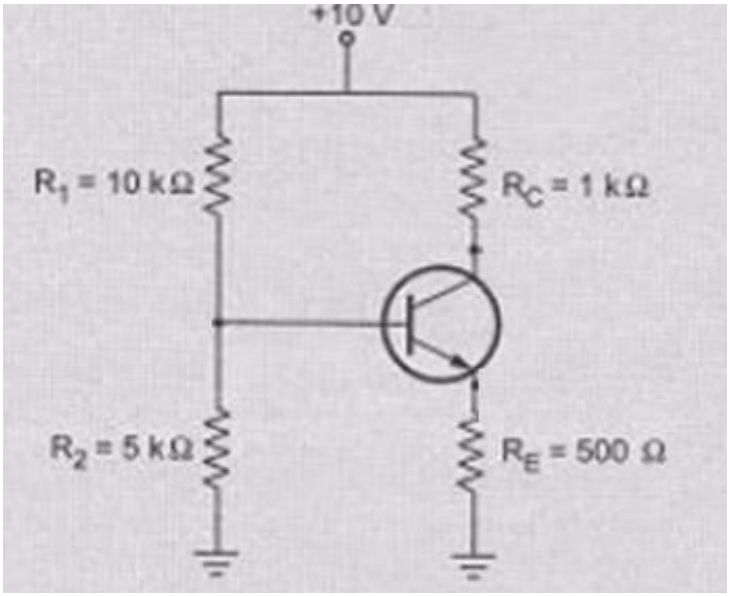
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

**Problem 1:**

For the given circuit β=100 for silicon transistor. Calculate $V_{CE}$ and $I_C$.




$$R_{TH} = \frac{10 * 5 * 10^6}{(10 + 5) * 10^3} = 3.33K\Omega$$

$$V_{TH} = \frac{10 * 5 * 10^3}{(10 + 5) * 10^3} = 3.33V$$

$$I_B = \frac{V_T - V_{BE}}{(R_B + (\beta + 1)R_E)} = \frac{3.33 - 0.7}{3.33 * 10^3 + 101 * 500} = 48.86\mu A$$

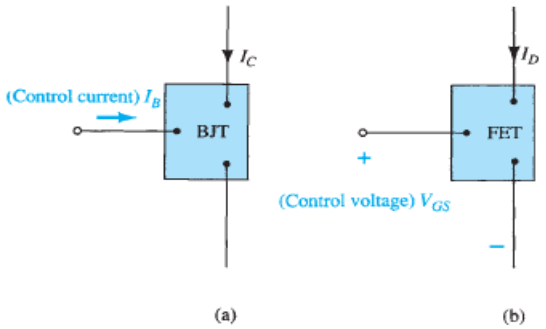
$$I_C = \beta I_B = 100 * 48.86 * 10^{-6} = 4.886mA$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 10 - 4.886 * 10^{-3} * (1 * 10^3 + 500) = 2.645V$$

# MODULE – 3

## FET (Field Effect Transistor)

**The BJT transistor is a current-controlled device as depicted in Fig. a, whereas the JFET transistor is a voltage-controlled device as shown in Fig. b.**




Current controlled Device  Voltage controlled Device

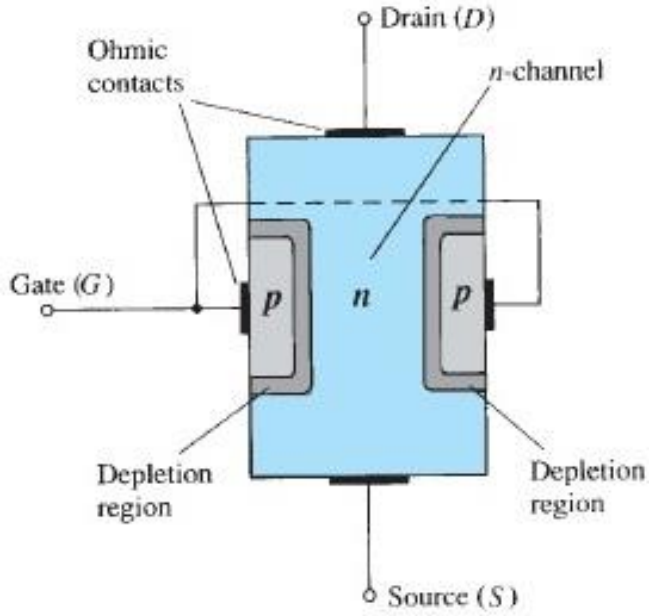
FET stands for field effect transistor because the output of the FETs is controlled by the supplied gate voltage. One of the most important characteristics of the FET is its high input impedance. The JFET transistor is a voltage-controlled device. FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

Two types of FETs are introduced here: the junction field-effect transistor (JFET) and the metal oxide semiconductor field-effect transistor (MOSFET). The MOSFET category is further broken down into depletion and enhancement types, which are both described. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design.

### CONSTRUCTION AND CHARACTERISTICS OF JFETs

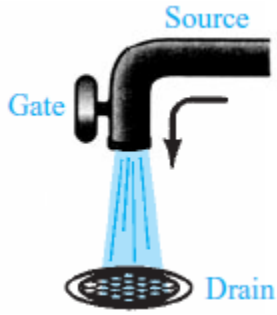
The JFET is a three-terminal device with one terminal capable of controlling the current between the other two. For the JFET transistor the n –channel device will be the prominent device, with paragraphs and sections devoted to the effect of using a p -channel JFET. The basic construction of the n -channel JFET is shown here. The major part of the structure is the n -type material, which forms the channel between the embedded layers of p -type material. The top of the n -type channel is connected through an ohmic contact to a terminal referred to as the drain (D), whereas the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S). The two p -type materials are connected together and to the gate (G) terminal. In essence, therefore, the drain and the source are connected to the ends of the n -type channel and the gate to the two layers of p -type material. In the absence of any applied potentials the JFET has two p – n junctions under

no-bias conditions. The result is a depletion region at each junction that resembles the same region of a diode under no-bias conditions. A depletion region is void of free carriers and is therefore unable to support conduction.




***Junction field-effect transistor (JFET)***

The "gate," through an applied signal (potential), controls the flow of charge to the "drain". The drain and source terminals are at opposite ends of the *n* -channel because the terminology is defined for electron flow.

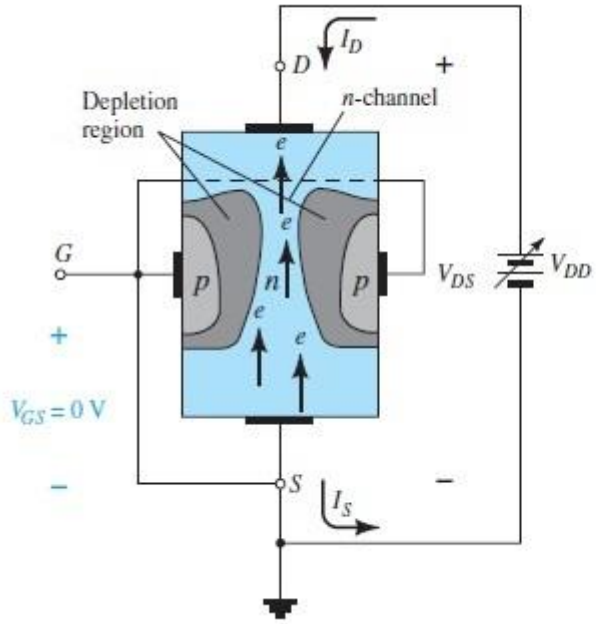



*Water analogy for the JFET control mechanism.*

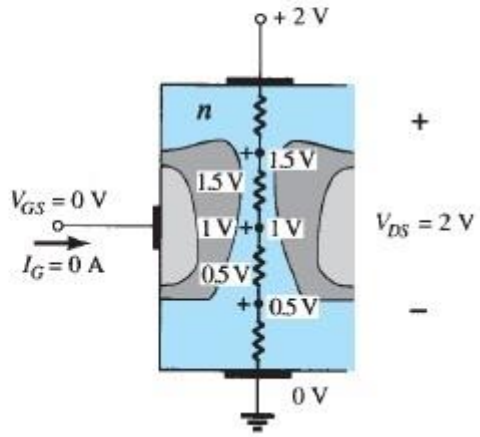
Water analogy of the above figure does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source, which establishes a flow of water (electrons) from the spigot (source). The "gate," through an applied signal (potential), controls the flow of water (charge) to the "drain." The drain and source terminals are at opposite ends of the *n* -channel as JFET because the terminology is defined for electron flow.

## $V_{GS}$= 0 V, $V_{DS}$ Some Positive Value

A positive voltage $V_{DS}$ is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and a source terminal at the same potential and a depletion region in the low end of each p–material. The instant the voltage $V_{DD}$ (=$V_{DS}$) is applied, the electrons are drawn to the drain terminal, establishing the conventional current $I_D$ with the defined direction as shown in figure. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D$ = $I_S$). The flow of charge is relatively uninhibited and is limited solely by the resistance of the n -channel between drain and source.



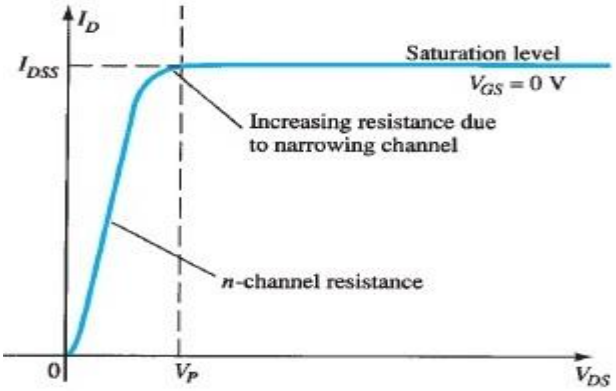

*(JFET at $V_{GS}$ = 0 V and $V_{DS}$> 0 V)*




***Varying reverse-bias potentials across the p–n junction of an n-channel JFET.***

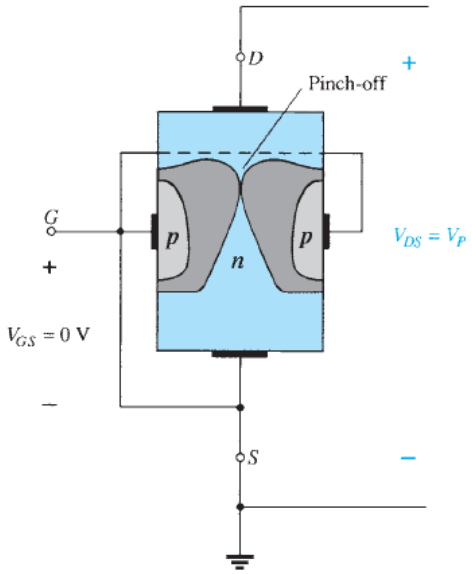
The depletion region is wider near the top of both p –type materials. As expressed in the diagram assuming a uniform resistance in the n -channel, we can break down the resistance of the channel into the divisions. The current $I_D$ will establish the voltage levels through the channel as indicated on the same figure. The result is that the upper region of the p -type material will be more reverse-biased compared to the lower region.

The fact that the p – n junction is reverse-biased for the length of the channel results in a gate current of zero amperes. The fact that $I_G$ = 0 A is an important characteristic of the JFET.



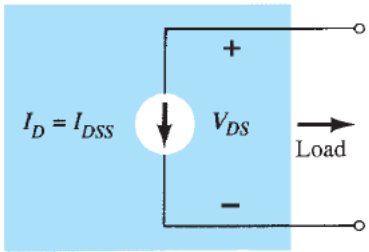

*$I_D$ versus $V_{DS}$ for $V_{GS}$ = 0 V.*

As the voltage $V_{DS}$ is increased from 0 V to a few volts, the current will increase as determined by Ohm's law. The relative straightness of the plot reveals that for the region of low values of $V_{DS}$, the resistance is essentially constant. As $V_{DS}$ increases and approaches a level referred to as $V_P$, the depletion regions will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If $V_{DS}$ is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as pinch-off will result. The level of $V_{DS}$ that establishes this condition is referred to as the pinch-off voltage and is denoted by $V_P$. In reality a very small channel still exists, with a current of very high density.




*Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).*

As $V_{DS}$ is increased beyond $V_P$, the region of close encounter between the two depletion regions increases in length along the channel, but the level of $I_D$ remains essentially the same. In essence, therefore, once $V_{DS} > V_P$ the JFET has the characteristics of a current source. The current is fixed at $I_D = I_{DSS}$, but the voltage $V_{DS} > V_P$ is determined by the applied load. $I_{DSS}$ is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > V_P$.

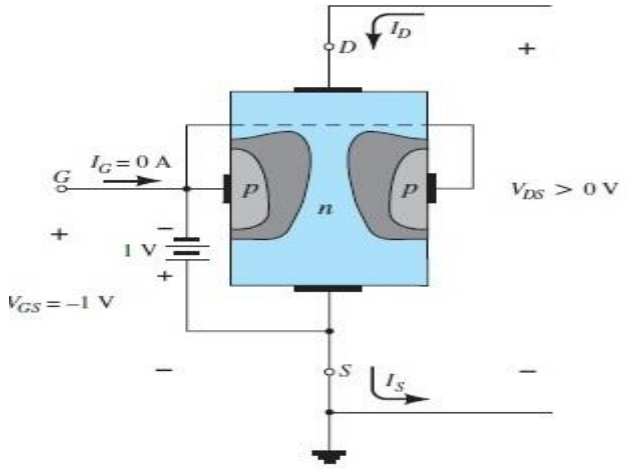



*Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.*

*$I_{DSS}$ is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0\ V$ and $V_{DS} > |V_P|$.*

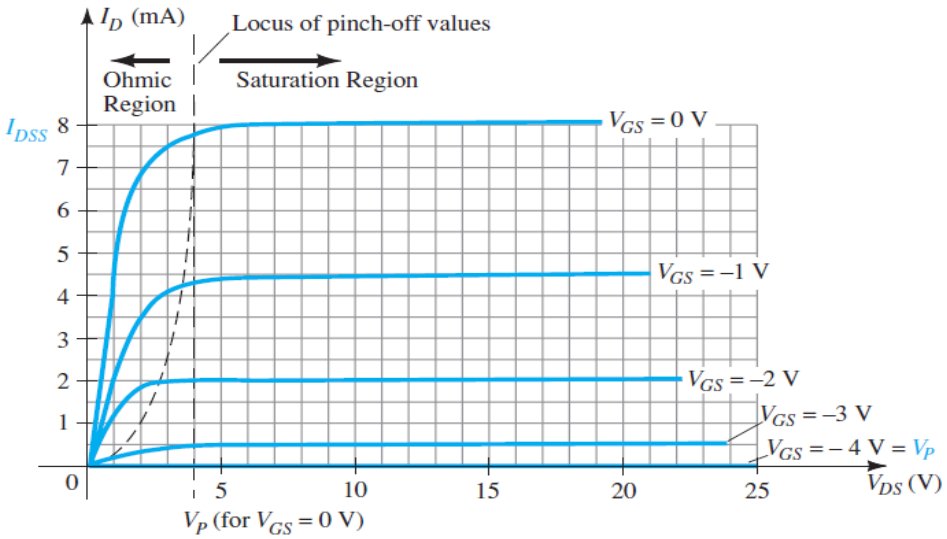
**$V_{GS} < 0$ V**

The voltage from gate to source, denoted $V_{GS}$, is the controlling voltage of the JFET. For the *n*-channel device the controlling voltage $V_{GS}$ is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.




*Application of a negative voltage to the gate of a JFET.*

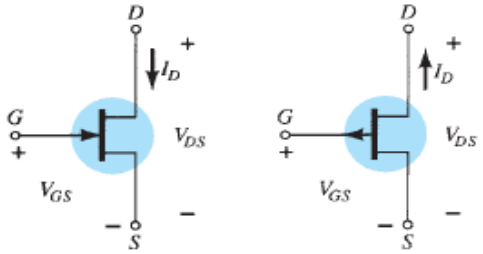
When a negative voltage is applied between the gate and source terminals the depletion layer width will be more due to reverse basing effect which was not present during $V_{GS} = 0$ V. As a result the channel becomes narrow and $I_D$ is reduced and it will continue to decrease as $V_{GS}$ is made more and more negative. Finally, for a fixed negative value of $V_{GS}$, the current becomes zero which is known as pinch off voltage $V_P$.




*n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.*

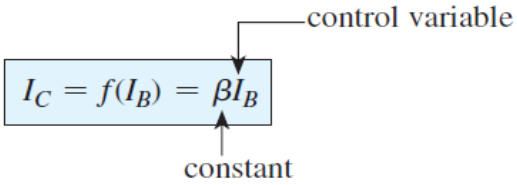
*The level of $V_{GS}$ that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with $V_P$ being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.*

The graphic symbols for the *n* -channel and *p* -channel JFETs are shown below. Note that the arrow is pointing in for the *n* -channel device to represent the direction in which $I_G$ would flow if the $p - n$ junction was forward-biased. For the *p* -channel device the only difference in the symbol is the direction of the arrow in the symbol.



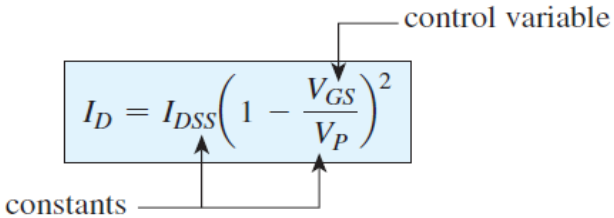

## TRANSFER CHARACTERISTICS

For the BJT transistor the output current $I_C$ and the input controlling current $I_B$ are related by beta, which was considered constant for the analysis to be performed. In equation form,




In Eq. a linear relationship exists between $I_C$ and $I_B$. Double the level of $I_B$ and $I_C$ will increase by a factor of two also.

Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between $I_D$ and $V_{GS}$ is defined by *Shockley's equation*




The squared term in the equation results in a nonlinear relationship between $I_D$ and $V_{GS}$, producing a curve that grows exponentially with decreasing magnitude of $V_{GS}$.

The current voltage relationship is given by the Shockley's equation,

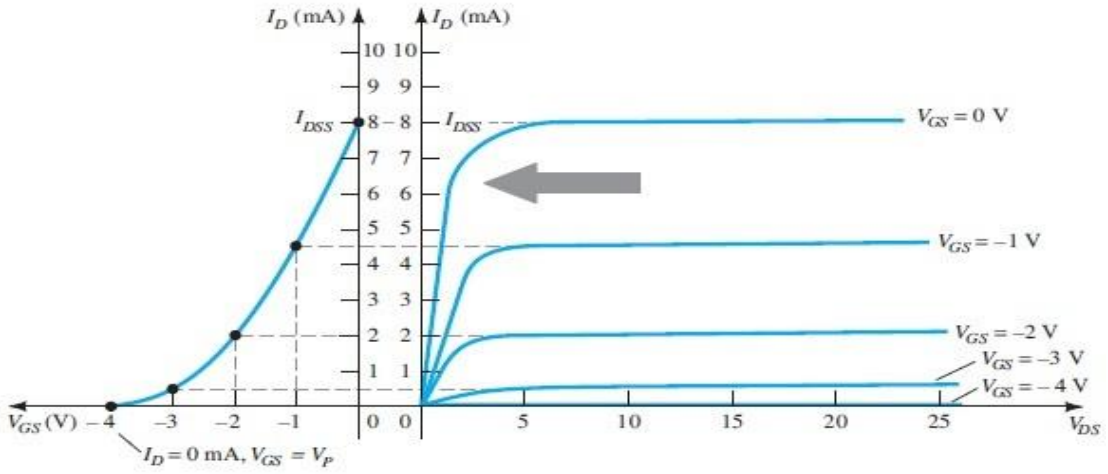
$$\mathbf{I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2}$$

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

The transfer curve can be obtained

1. using Shockley's equation
2. or from the output characteristics

**From the output characteristics**




*Obtaining the transfer curve from the drain characteristics.*

In review:

$$\text{When } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS}$$

When $V_{GS} = V_P = -4$ V, the drain current is 0 mA, defining another point on the transfer curve. That is:

$$\text{When } V_{GS} = V_P, \quad I_D = 0\text{ mA}$$

**Using Shockley's equation**

$$\mathbf{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

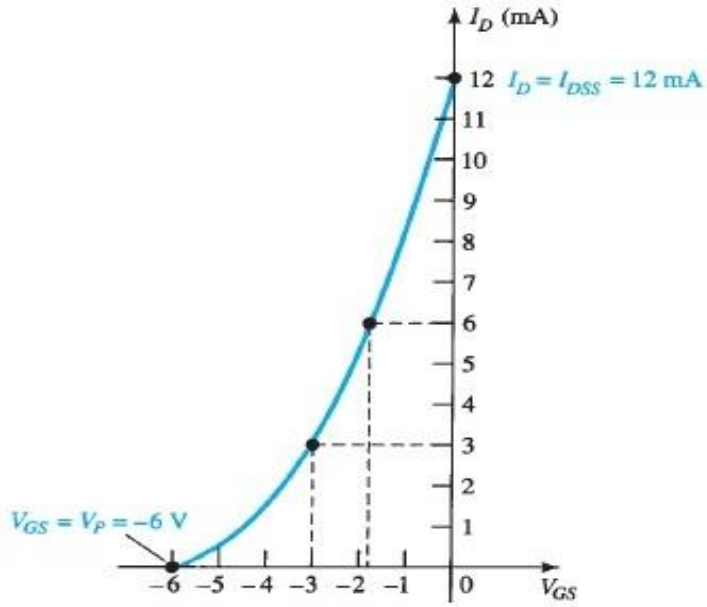
| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $I_{DSS}$ |
| $0.3V_P$ | $\frac{I_{DSS}}{2}$ |
| $0.5V_P$ | $\frac{I_{DSS}}{4}$ |
| $V_P$ | 0 |

**Problem: -**

Sketch the transfer curve defined by $I_{DSS}$ = 12 mA and $V_P = -6$ V.

**Ans**: -

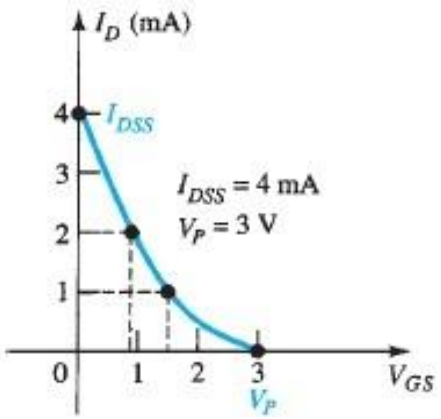
| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $I_{DSS} = 12$ |
| $0.3V_P = -1.8$ | $\frac{I_{DSS}}{2} = 6$ |
| $0.5V_P = -3$ | $\frac{I_{DSS}}{4} = 3$ |
| $V_P = -6$ | 0 |



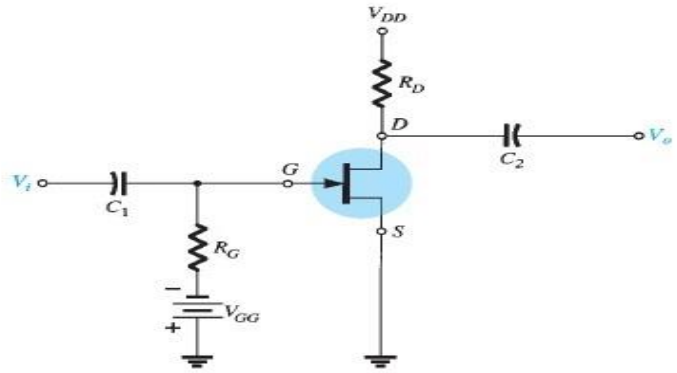

**problem: -** Sketch the transfer curve of a P-channel JFET defined by $I_{DSS}$ = 4 mA and $V_P = 3$ V

**Ans**:-

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $I_{DSS} = 4$ |
| $0.3V_P = 0.9$ | $\frac{I_{DSS}}{2} = 2$ |
| $0.5V_P = 1.5$ | $\frac{I_{DSS}}{4} = 1$ |
| $V_P = 3$ | 0 |

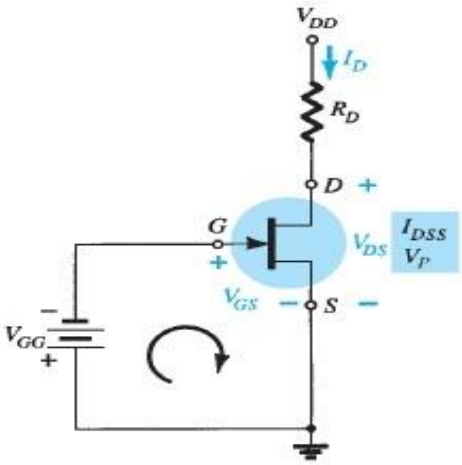


## FIXED-BIAS CONFIGURATION




**Source-Gate Loop**

The dc bias network of the Source-Gate loop of the fixed-bias Configuration is shown here.




Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction,

$$-V_{GG} - V_{GS} = 0$$

$$\mathbf{V_{GS} = -V_{GG}}$$

Since $V_{GG}$ is a fixed dc supply, the voltage $V_{GS}$ is fi
designation" fixed-bias configuration."

The resulting level of drain current $I_D$ is now controlled

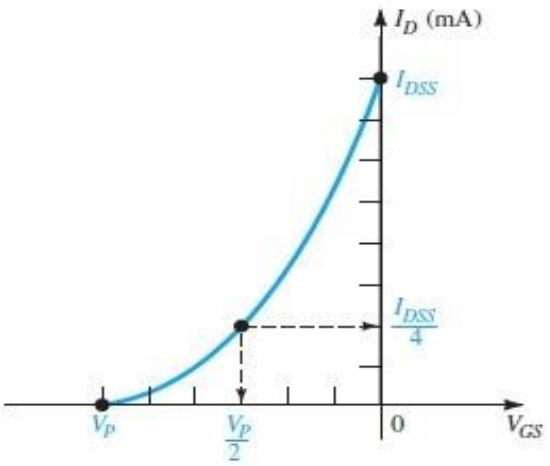
$$\mathbf{I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2}$$

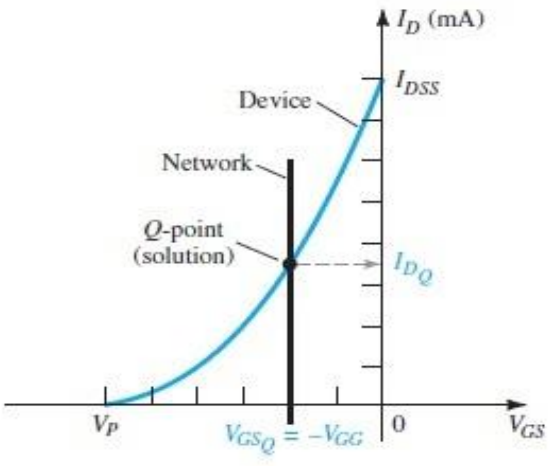
Since $V_{GS}$ is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of $I_D$ is calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

The quotient point can be calculated through graphical analysis. On the transfer characteristic curve when the load line will be drawn it will intersect the characteristic curve at the Q-point.

From the Shockley's equation the relation between $I_D$ and $V_{GS}$ is determined which is used to draw the transfer characteristic of the JFET.

| $\mathbf{V_{GS}}$**(V)** | $\mathbf{I_D}$**(mA)** |
|---|---|
| 0 | $I_{DSS}$ |
| $0.3V_P$ | $\frac{I_{DSS}}{2}$ |
| $0.5V_P$ | $\frac{I_{DSS}}{4}$ |
| $V_P$ | 0 |




**Drain–Source Loop**

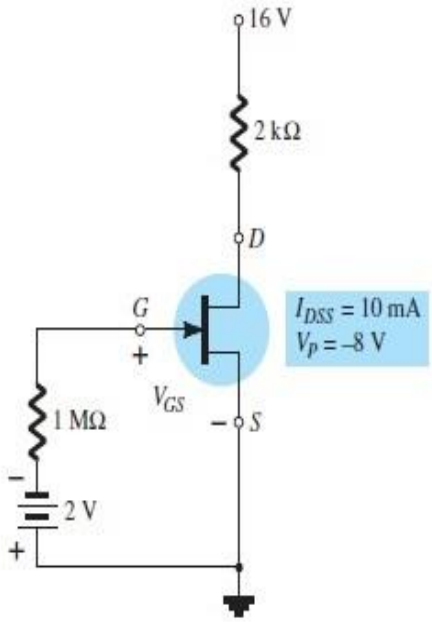
Applying Kirchhoff's voltage law in the clockwise direction around the collector-emitter loop will result in the following:

$V_{DD} - I_D R_D - V_{DS} = 0$

$\mathbf{V_{DS} = V_{DD} - I_D R_D}$

**Problem :-**

Determine $I_{DQ}$ , $V_{GSQ}$ , $V_{DS}$ , $V_D$ , $V_G$ , $V_S$ for the fixed bias circuit with $V_{DD}$=16V, $V_{GG} = 2V$ , $R_G$ =1M , $R_D$ =2K , $I_{DSS} = 10mA$ , $V_P = -8V$ .




**ans:-**

**Mathematical method :-**

$V_{GS} = -V_{GG}$

$\mathbf{V_{GSQ} = -2V}$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$I_D = 10m * \left(1 - \frac{-2}{-8}\right)^2$

$\mathbf{I_{DQ} = 5.625mA}$

$V_{DS} = V_{DD} - I_D R_D$

$V_{DS} = 16 - 5.625mA * 2K$

$\mathbf{V_{DS}}$ **=4.75V**

$V_G = V_{GS}$

$\mathbf{V_G = -2V}$

$V_D = V_{DS}$

$\mathbf{V_D = 4.75V}$

$\mathbf{V_S = 0}$

**Graphical method :-**

To draw the transfer characteristic, we need the Shockley's equation:

$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$

Here $I_{DSS} = 10$ mA and $V_P = -8V$

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $I_{DSS} = 10$ |
| $0.3V_P = -2.4$ | $\frac{I_{DSS}}{2}$ =5 |
| $0.5V_P = -4$ | $\frac{I_{DSS}}{4}$ =2.5 |
| $V_P = -8$ | 0 |

Again, as it is a fixed bias circuit so the input loop gives $V_{GS} = -V_{GG}$, which intersects the transfer characteristic at the Q-point with $V_{GS} = -2V$ and $I_D = 5.6mA$ .

Therefore,

$\mathbf{V_{GSQ} = -2V}$

$\mathbf{I_{DQ} = 5.6mA}$

$V_{DS} = V_{DD} - I_D R_D$

$V_{DS} = 16 - 5.6mA * 2K$

$\mathbf{V_{DS}}$ **=4.8V**

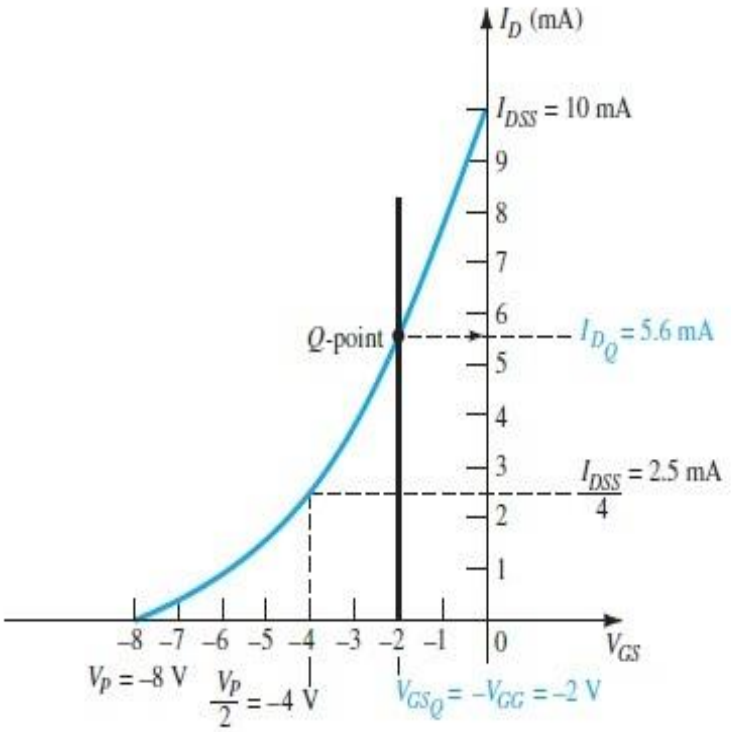
$V_G = V_{GS}$

$\mathbf{V_G = -2V}$

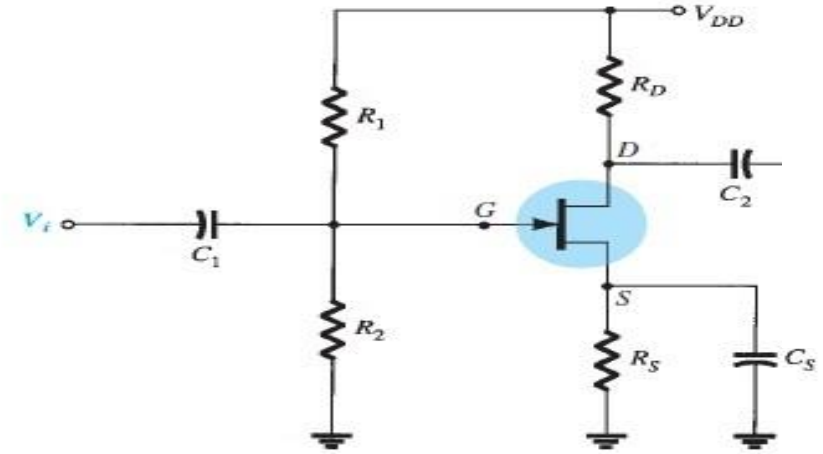
$V_D = V_{DS}$

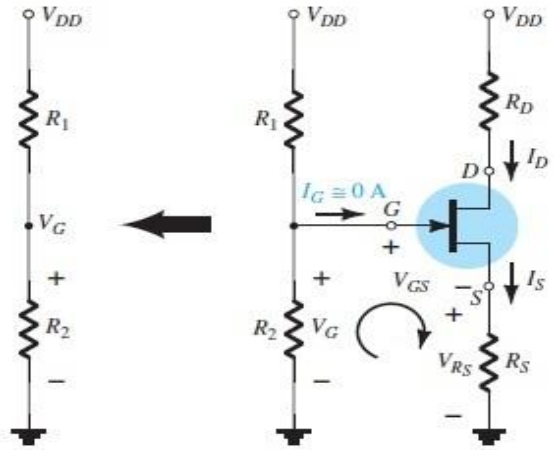
$\mathbf{V_D = 4.8V}$

$\mathbf{V_S = 0}$



## VOLTAGE DIVIDER BIAS CONFIGURATION




**Source-Gate Loop**

The source $V_{DD}$ was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since $I_G$ = 0 A, Kirchhoff's current law requires that $I_{R1} = I_{R2}$, and the series equivalent circuit appearing to the left of the figure can be used to find the level of $V_G$ . The voltage $V_G$ , equal to the voltage across $R_2$, can be found using the Voltage-divider rule.

$$\mathbf{V_G = \frac{V_{DD} * R_2}{R_1 + R_2}}$$

Applying Kirchhoff's voltage law to the input loop

$$V_G - V_{GS} - I_D R_S = 0$$

$$\mathbf{V_{GS} = V_G - I_D R_S}$$

The resulting level of drain current $I_D$ is now controlled by Shockley's equation: $\mathbf{I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2}$

Both equations relate the same two variables, $I_D$ and $V_{GS}$, permitting either a mathematical or a graphical solution. Since, $V_{GS}$ is a function of the output current $I_D$ for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of $I_D$ is calculated.

Mathematical solution could be obtained simply by substituting ($V_{GS} = V_G - I_D R_S$) into Shockley's equation as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

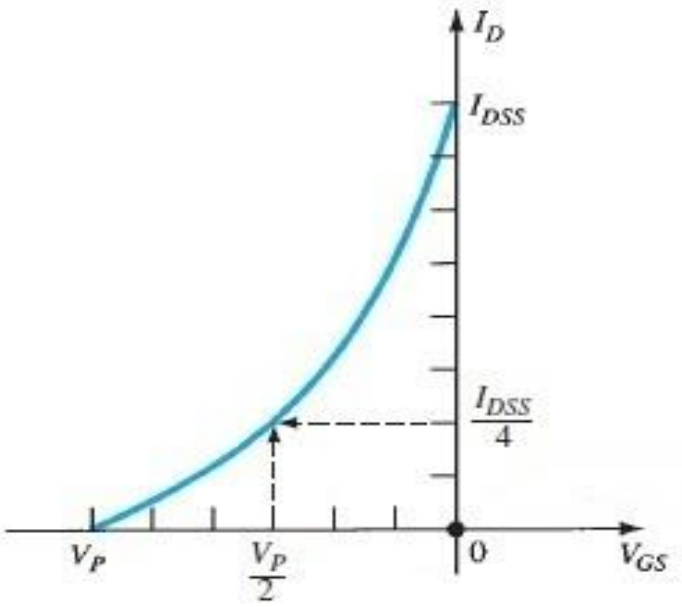
$$I_D = I_{DSS}\left(1 - \frac{V_G - I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, we obtain a quadratic equation which can be solved to get the value of $I_D$ and $V_{GS}$ .

The quotient point can be calculated through graphical analysis. On the transfer characteristic curve when the load line will be drawn it will intersect the characteristic curve at the Q-point.

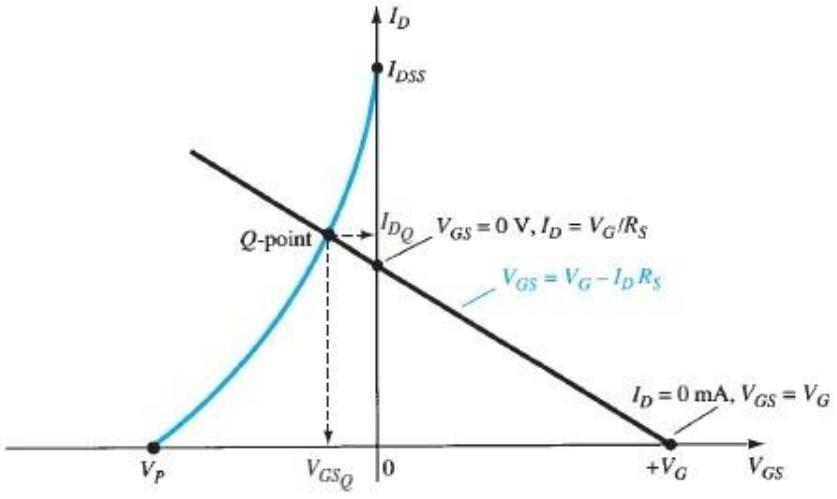
From the Shockley's equation the relation between $I_D$ and $V_{GS}$ is determined which is used to draw the transfer characteristic of the JFET.

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $I_{DSS}$ |
| $-0.3V_P$ | $\frac{I_{DSS}}{2}$ |
| $-0.5V_P$ | $\frac{I_{DSS}}{4}$ |
| $V_P$ | 0 |



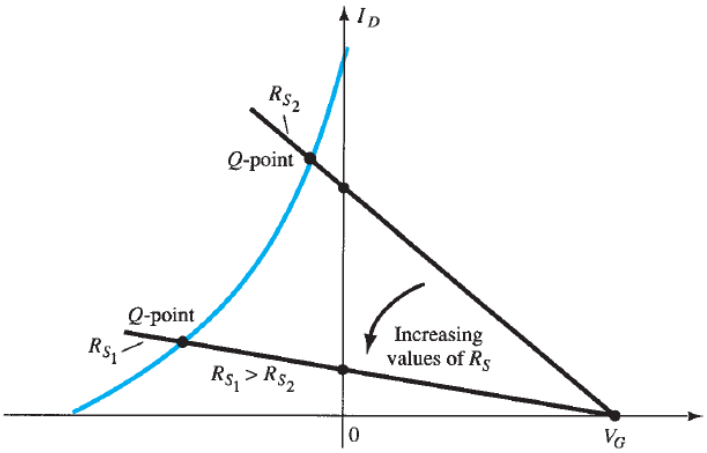

From the input KVL equation the load line c
equation $V_{GS} = V_G - I_D R_S$,

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $\frac{V_G}{R_S}$ |
| $V_G$ | 0 |




*Sketching the network equation for the voltage-divider configuration.*

*Increasing values of $R_S$ result in lower quiescent values of $I_D$ and declining values of $V_{GS}$.*




*Effect of $R_S$ on the resulting Q-point.*

**Drain–Source Loop**

Applying Kirchhoff's voltage law in the clockwise direction around the collector-emitter loop will result in the following:

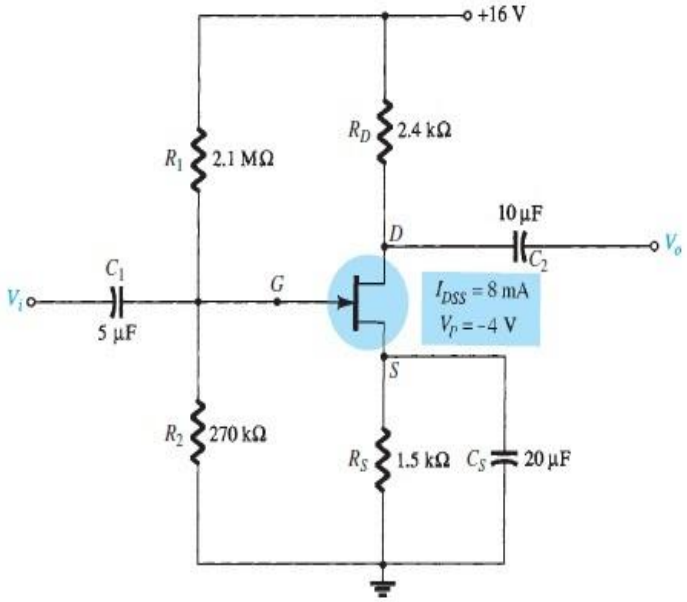
$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$\mathbf{V_{DS} = V_{DD} - I_D(R_D + R_S)}$

**Problem :-**

Determine $I_{DQ}$ , $V_{GSQ}$ , $V_{DS}$ , $V_D$ , $V_{DG}$ , $V_S$ for the voltage divider bias circuit with $V_{DD}$=16V, $R_1$ = 2.1M , $R_2 = 270K$ , $R_D$ =2.4K , $R_S$ =1.5K , $I_{DSS} = 8mA$ , $V_P = -4V$ .

**ans**:-




**Mathematical method :-**

$V_{GS} = V_G - I_D R_S$

$V_G = \dfrac{V_{DD} * R_2}{R_1 + R_2}$

$V_G = \dfrac{16 * 270K}{2.1M + 270K}$

$\mathbf{V_G = 1.82\ V}$

$V_{GS} = 1.82 - I_D(1.5K)$ ----------(1)

$I_D = I_{DSS}(1 - \dfrac{V_{GS}}{V_P})^2$

$I_D = 8m\left(1 - \dfrac{V_{GS}}{-4}\right)^2$ ----------(2)

Solving equation-1and 2 we get,

$\mathbf{V_{GSQ} = -1.8V}$
$\mathbf{I_{DQ} = 2.4mA}$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$
$V_{DS} = 16 - 2.4\text{mA} * (2.4\text{K} + 1.5\text{K})$
$\mathbf{V_{DS}}$ **=6.64V**

$V_S = I_D R_S$
$V_S = 2.4\text{mA} * 1.5\text{K}$
$\mathbf{V_S = 3.6V}$

$V_D = V_{DS} + V_S$
$V_D = 6.64 + 3.6$
$\mathbf{V_D = 10.24\ V}$

$V_{DG} = V_D - V_G$
$V_{DG} = 10.24 - 1.82$
$\mathbf{V_{DG} = 8.42\ V}$

**Graphical method :-**

To draw the transfer characteristic we need the Shockley's equation:

$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$

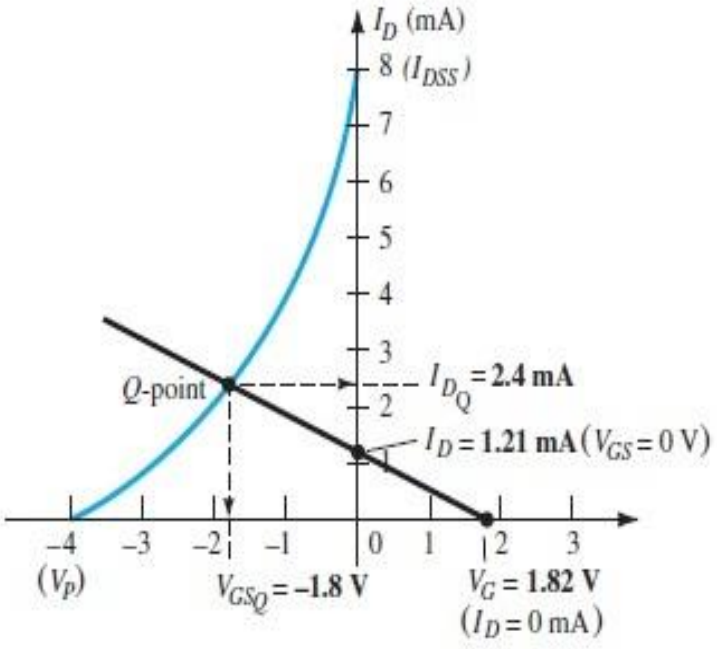
Here $I_{DSS} = 8$ mA and $V_P = -4V$

| $\mathbf{V_{GS}}$**(V)** | $\mathbf{I_D}$**(mA)** |
|---|---|
| 0 | $I_{DSS} = 8$ |
| $0.3V_P = -1.2$ | $\frac{I_{DSS}}{2}$ =4 |
| $0.5V_P = -2$ | $\frac{I_{DSS}}{4}$ =2 |
| $V_P = -4$ | 0 |

From the input loop of the Voltage divider bias circuit we get

$V_{GS} = V_G - I_D R_S$ ,

| $\mathbf{V_{GS}}$**(V)** | $\mathbf{I_D}$**(mA)** |
|---|---|
| 0 | $\frac{V_G}{R_S} = 1.21$ |
| 1.82 | 0 |




which intersects the transfer characteristic at the Q-point with $V_{GS} = -1.8V$ and $I_D = 2.4mA$. Therefore,

$\mathbf{V_{GSQ} = -1.8V}$
$\mathbf{I_{DQ} = 2.4mA}$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$
$V_{DS} = 16 - 2.4mA * (2.4K + 1.5K)$
$\mathbf{V_{DS} = 6.64V}$

$V_S = I_D R_S$
$V_S = 2.4mA * 1.5K$
$\mathbf{V_S = 3.6V}$

$V_D = V_{DS} + V_S$
$V_D = 6.64 + 3.6$
$\mathbf{V_D = 10.24\ V}$

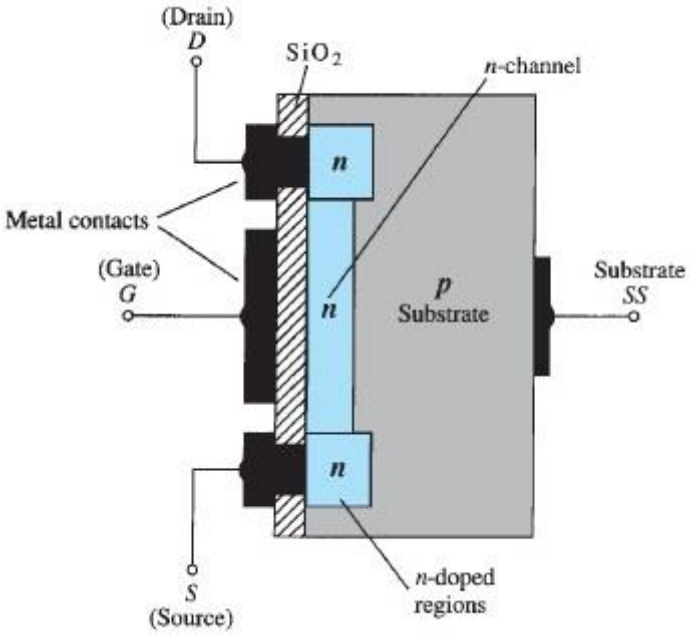
$V_{DG} = V_D - V_G$
$V_{DG} = 10.24 - 1.82$
$\mathbf{V_{DG} = 8.42\ V}$

## MOSFETs

MOSFET stands for metal oxide semiconductor field effect transistor where on a substrate drain, gate and source are formed. MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation. Since there are differences in the characteristics and operation of different types of MOSFET, they are covered in separate sections.

**DEPLETION-TYPE MOSFETs**

The basic construction of the n -channel depletion-type MOSFET starts with a slab of p -type material known as substrate which is formed from a silicon base. It is the foundation on which the device is constructed. The source and drain terminals are connected through metallic contacts to n -doped regions linked by an n -channel. The gate is also connected to a metal contact surface but remains insulated from the n -channel by a very thin silicon dioxide (SiO2) layer. SiO2 is a type of insulator referred to as a dielectric, which sets up opposing electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO2 layer is an insulating layer means that: There is no direct electrical connection between the gate terminal and the channel of a MOSFET.




***n-Channel depletion-type MOSFET.***

The input resistance of a MOSFET is usually more than that of a typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. Because of the very high input impedance, the gate current $I_G$ is essentially 0A for dc biased configurations.

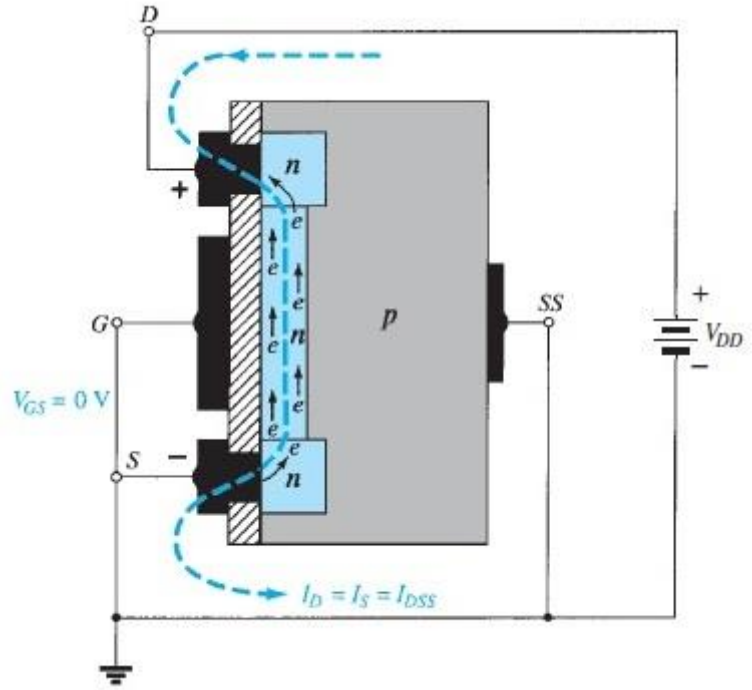
The reason for the label metal–oxide–semiconductor FET is now fairly obvious: metal for the drain, source, and gate connections; oxide for the silicon dioxide insulating layer; and semiconductor for the basic structure on which the n-type and p-type regions are diffused. The insulating layer between the gate and the channel has resulted in another name for the device: insulated-gate FET, or IGFET.

**Basic Operation and Characteristics**

**$V_{GS}$= 0 V, $V_{DS}$ Some Positive Value**

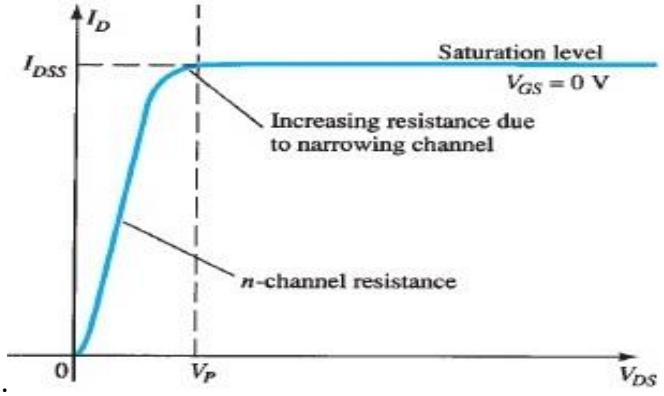
A positive voltage $V_{DS}$ is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and a source terminal at the same potential and a depletion region in the low end of each p–material. The instant the voltage $V_{DD}$ (=$V_{DS}$) is applied, the electrons are drawn to the drain terminal, establishing

the conventional current $I_D$ with the defined direction as shown in figure. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). The flow of charge is relatively uninhibited and is limited solely by the resistance of the n-channel between drain and source. The fact that there is an insulator between the gate and the channel, so no current is flowing from the gate terminal making $I_G = 0A$.



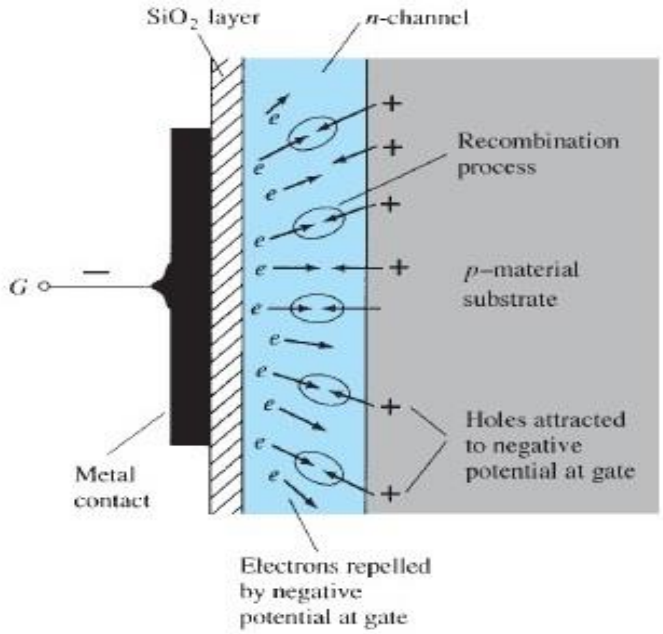

***(n-Channel depletion-type MOSFET with $V_{GS}$ = 0 V and applied voltage $V_{DD}$)***

As the voltage $V_{DS}$ is increased from 0 V to a few volts, the current will increase as determined by Ohm's law. The relative straightness of the plot reveals that for the region of low values of $V_{DS}$, the resistance is essentially constant. As $V_{DS}$ increases and approaches a level referred to as $V_P$, the depletion regions will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If $V_{DS}$ is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as pinch-off will result. The level of $V_{DS}$ that establishes this condition is referred to as the pinch-off voltage and is denoted by $V_P$. In reality a very small channel still exists, with a current of very high density.



**$V_{GS}$ < 0 V**

The voltage from gate to source, denoted $V_{GS}$, is the controlling voltage of the JFET. For the *n*-channel device the controlling voltage $V_{GS}$ is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.




***Reduction in free carriers in a channel due to a negative potential at the gate terminal.***

When a negative voltage is applied between the gate and source terminals the negative gate voltage will repel the charge carriers(electrons) present in the channel, which makes the channel narrow there by reducing the drain current and it will continue to decrease as $V_{GS}$ is made more and more negative. Finally, for a fixed negative value of $V_{GS}$, the current becomes zero which is known as pinch off voltage $V_P$.

**$V_{GS}$ > 0 V**

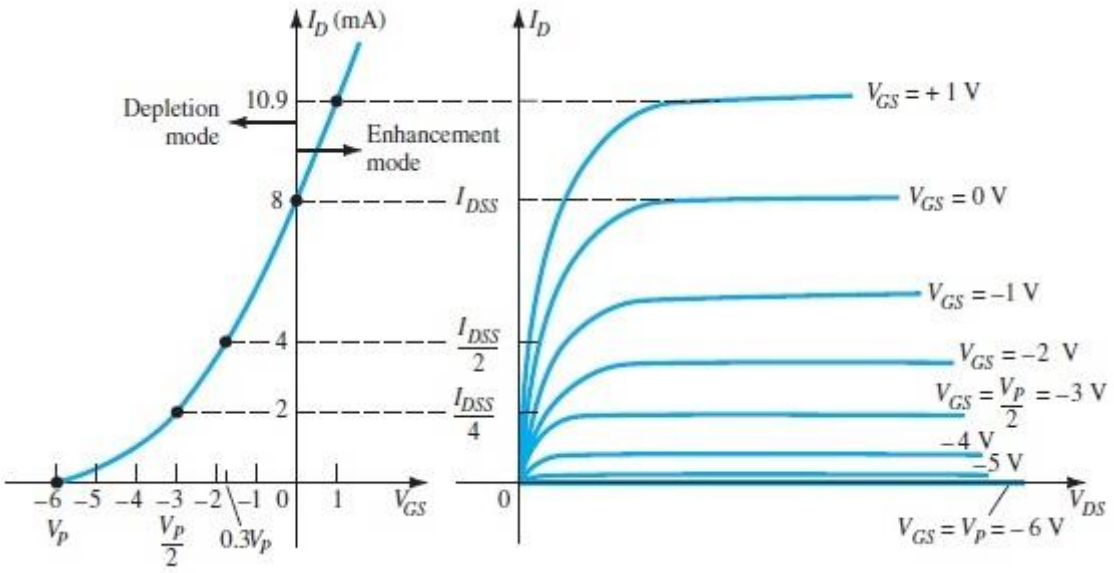
For positive values of $V_{GS}$, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. below reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the $V_{GS}$=0 V and $V_{GS}$ = +1 V curves is a clear indication of how much the current has increased for the 1-V change in $V_{GS}$. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device the application of a voltage $V_{GS}$ = +4 V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has **"enhanced"** the level of free carriers in the channel compared to that encountered with $V_{GS}$=0V. For this reason, the region of positive gate voltages on the drain or transfer characteristics is often referred to as the ***enhancement region,*** with the region between cut-off and the saturation level of $I_{DSS}$ referred to as the ***depletion region***.

The current voltage relationship is given by the Shockley's equation,

$$\mathbf{I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2}$$

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

| $\mathbf{V_{GS}(V)}$ | $\mathbf{I_D(mA)}$ |
|---|---|
| 0 | $I_{DSS}$ |
| $0.3V_P$ | $\frac{I_{DSS}}{2}$ |
| $0.5V_P$ | $\frac{I_{DSS}}{4}$ |
| $V_P$ | 0 |

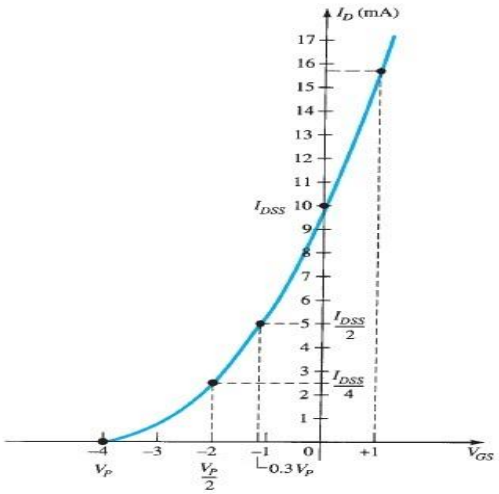



***Drain and transfer characteristics for an n-channel depletion-type MOSFET.***

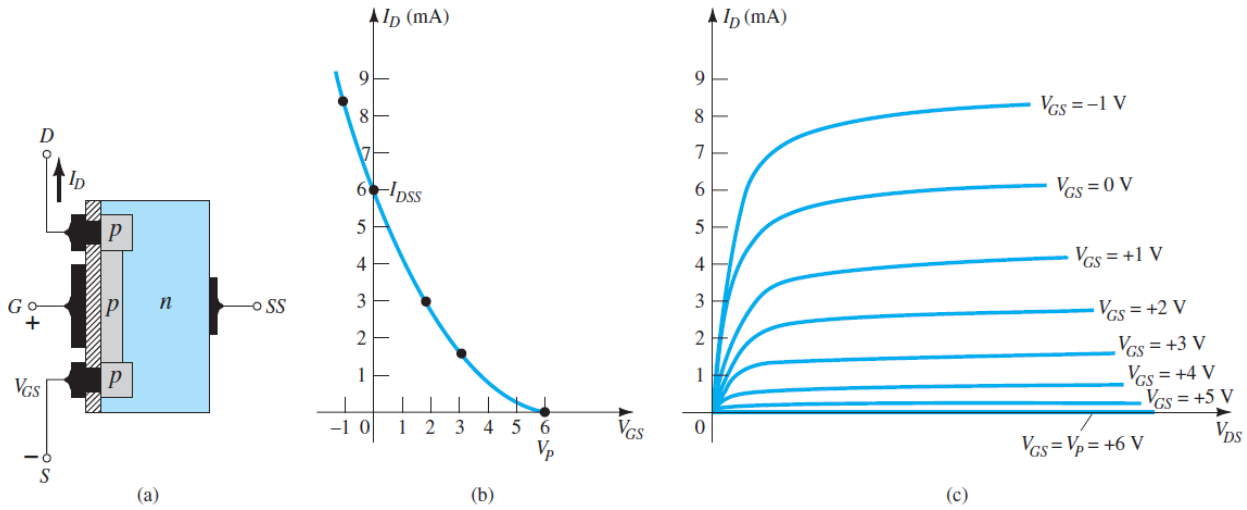
**Problem: -** Sketch the transfer characteristics for an ***n*-channel depletion-type MOSFET** with $\mathbf{I_{DSS} = 10\ mA}$ **and** $\mathbf{V_P = -4V}$**.**

**Ans: -**

| $\mathbf{V_{GS}(V)}$ | $\mathbf{I_D(mA)}$ |
|---|---|
| +1 | 15.63 |
| 0 | $I_{DSS} = 10$ |
| $0.3V_P = -1.2$ | $\frac{I_{DSS}}{2} = 5$ |
| $0.5V_P = -2$ | $\frac{I_{DSS}}{4} = 2.5$ |
| $V_P = -4$ | 0 |

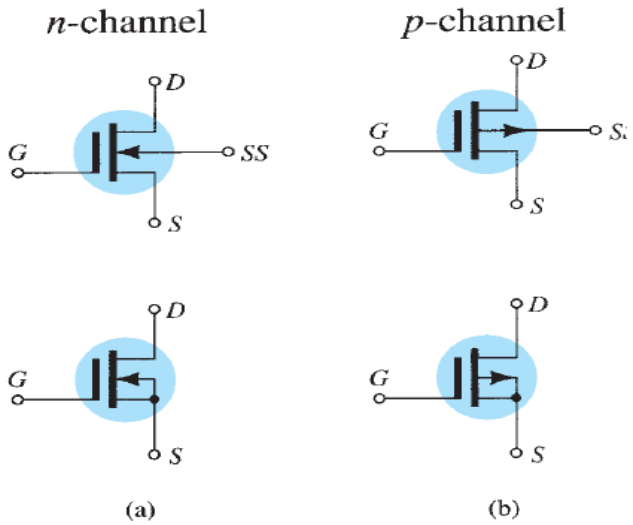


## *p* -Channel Depletion-Type MOSFET




***(p-Channel depletion-type MOSFET with $I_{DSS}$ = 6mA and $V_P$ = 6 V)***

The graphic symbols for the *n* -channel and *p* -channel JFETs are shown below. Note that the arrow is pointing in for the *n* -channel device to represent the direction in which $I_G$ would flow if the *p* – *n* junction was forward-biased. For the *p* -channel device the only difference in the symbol is the direction of the arrow in the symbol.




***Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.***

## BIASING IN DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. **The primary difference**

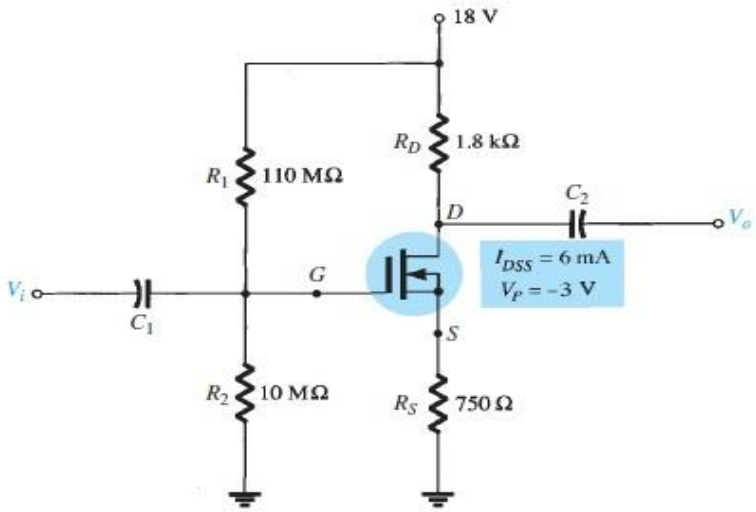
**between the two is the fact that depletion-type MOSFETs permit operating points with positive values of $V_{GS}$ and levels of $I_D$ that exceed $I_{DSS}$.** In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

**Problem:**

Determine $I_{DQ}, V_{GSQ}, V_{DS}$ for the voltage divider bias circuit with $V_{DD}$=18V, $R_1$ =110M, $R_2 = 10M$, $R_D$ =1.8K , $R_S$=750K , $I_{DSS} = 6mA$, $V_P = -3V$ .

**ans:-**

**Mathematical method :-**




$$V_{GS} = V_G - I_D R_S$$

$$V_G = \frac{V_{DD} * R_2}{R_1 + R_2}$$

$$V_G = \frac{18 * 10M}{110M + 10M}$$

$$\mathbf{V_G = 1.5\ V}$$

$$V_{GS} = 1.5 - I_D(750) \text{ ----------(1)}$$

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

$$I_D = 6m\left(1 - \frac{V_{GS}}{-3}\right)^2 \text{ ----------(2)}$$

Solving equation-1and 2 we get,

$$\mathbf{V_{GSQ} = -0.8V}$$

$$\mathbf{I_{DQ} = 3.1mA}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)\ V_{DS} = 18 - 3.1mA * (1.8K + 750)$$

**$V_{DS}$ = 10.1V**

**Graphical method :-**

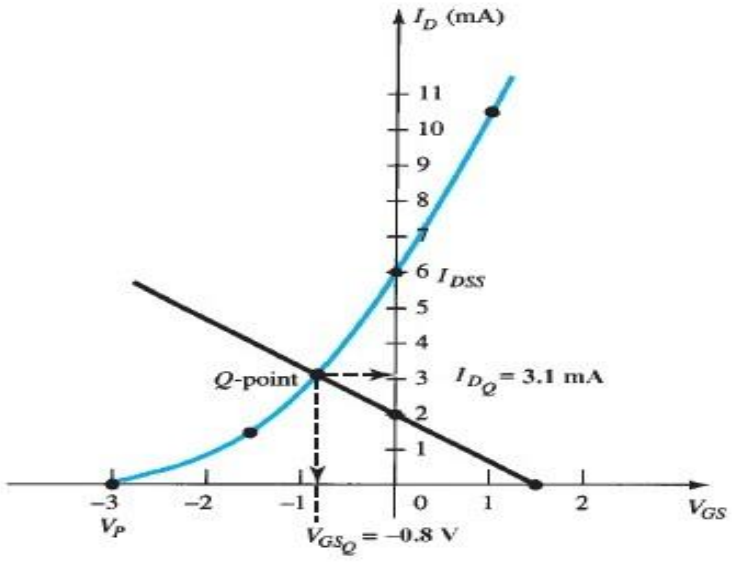
To draw the transfer characteristic we need the Shockley's equation:

$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$ Here $I_{DSS} = 6$ mA and $V_P = -3V$

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $I_{DSS} = 6$ |
| $0.3V_P = -0.9$ | $\frac{I_{DSS}}{2}$ =3 |
| $0.5V_P = -1.5$ | $\frac{I_{DSS}}{4}$ =1.5 |
| $V_P = -3$ | 0 |
| +1 | 10.67 |

From the input loop of the Voltage divider bias circuit we get $V_{GS} = V_G - I_D R_S$,

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $\frac{V_G}{R_S} = 2$ |
| 1.5 | 0 |




which intersects the transfer characteristic at the Q-point with $V_{GS} = -0.8V$ and $I_D = 3.1mA$. Therefore,

$\mathbf{V_{GSQ} = -0.8V}$

$\mathbf{I_{DQ} = 3.1mA}$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$V_{DS} = 18 - 3.1mA * (1.8K + 750)$

**$V_{DS}$ = 10.1V**

**Problem: -**

Determine $I_{DQ}$ , $V_{GSQ}$ , $V_{DS}$ for the self-bias circuit with $V_{DD}$=20V, $R_G$ =1M, $R_D$ =6.2K, $R_S$ =2.4K, $I_{DSS} = 8m$

**ans:-**

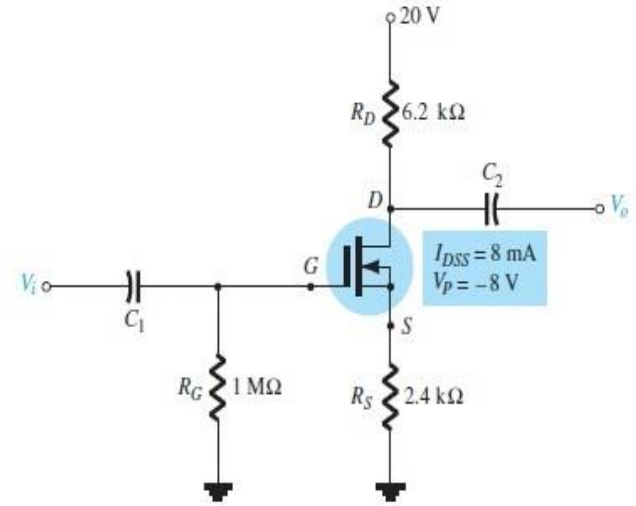
**Mathematical method :-**

$V_{GS} = -I_D R_S$

$V_{GS} = -I_D * (2.4K)$ ----------(1)

$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$

$I_D = 8m\left(1 - \frac{V_{GS}}{-8}\right)^2$ ----------(2)



Solving equation 1 and 2 we get,

$\mathbf{V_{GSQ} = -4.3V}$
$\mathbf{I_{DQ} = 1.7mA}$

$V_D = V_{DD} - I_D(R_D)$
$V_D = 20 - 1.7\text{mA} * (6.2\text{K})$
**$V_D$ =9.46V**

**Graphical method :-**

To draw the transfer characteristic we need the Shockley's equation:

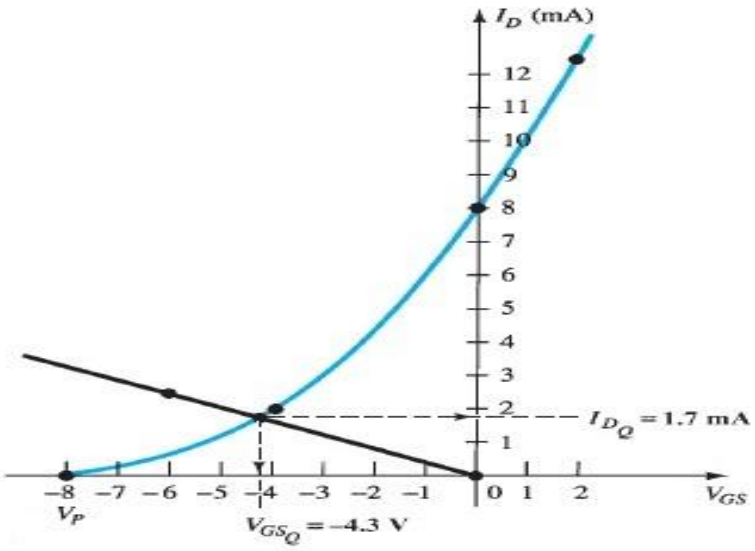
$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

Here $I_{DSS} = 8$ mA and $V_P = -6V$

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | $I_{DSS} = 8$ |
| $-0.3V_P = -1.8$ | $\frac{I_{DSS}}{2}$ =4 |
| $-0.5V_P = -3$ | $\frac{I_{DSS}}{4}$ =2 |
| $V_P = -6$ | 0 |
| +2 | 12.5 |

Again, as it is a self-bias circuit so the input loop gives $V_{GS} = -I_D R_S$ ,

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 0 | 0 |
| $-6$ | 2.5 |



which intersects the transfer characteristic at the Q-point with $V_{GS} = -4.3V$ and $I_D = 1.7mA$

Therefore,

$\mathbf{V_{GSQ} = -4.3V}$
$\mathbf{I_{DQ} = 1.7mA}$

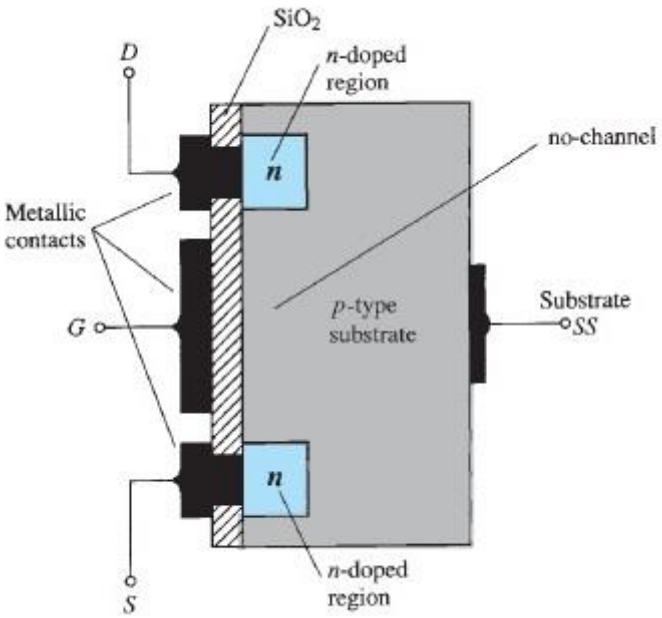
$V_D = V_{DD} - I_D(R_D)$
$V_D = 20 - 1.7mA * (6.2K)$
**$V_D$ =9.46**

## ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from D-MOSFET and JFET.

### Basic Construction

A slab of p -type material is formed from a silicon base and is again referred to as the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions, but there is no channel between the two n -doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs. The SiO2 layer is present to isolate the gate metallic platform from the region between the drain and source.



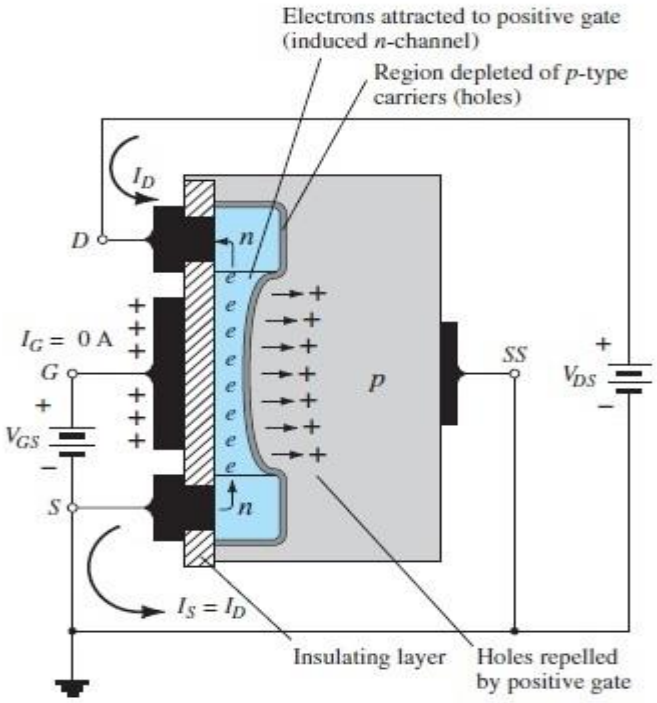

***(n-Channel enhancement-type MOSFET.)***

### Basic Operation and Characteristics

If $V_{GS}$ is set at 0 V and a voltage applied between the drain and the source of the device, then no current will flow from drain to source due to the absence of an channel. When $V_{DS}$and $V_{GS}$ have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source. The positive potential at the gate will

pressure the holes in the p-substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p-substrate. The result is a depletion region near the SiO2 insulating layer void of holes. However, the minority carriers i.e. electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO2 layer. As $V_{GS}$ increases in magnitude, the concentration of electrons near the SiO2 surface increases and finally creates a channel between drain and source. The level of $V_{GS}$ that results in the significant increase in drain current is called the "threshold voltage" and is given the symbol $V_T$ .The level of $V_{GS}$ that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol $V_T$. On specification sheets it is referred to as $V_{GS(Th)}$, although $V_T$ is less unwieldy and will be used in the analysis to follow.

Since the channel is non-existent with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET. Both depletion- and enhancement type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.




***(Channel formation in the n-channel enhancement-type MOSFET.)***

As $V_{GS}$ is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold $V_{GS}$ constant and increase the level of $V_{DS}$, the drain current will eventually reach a saturation
level and the potential difference between drain and gate will start to reduce. But to have the channel minimum voltage requirement is $V_T$.

So $V_{DG} = V_T$

$V_D - V_G = V_T$

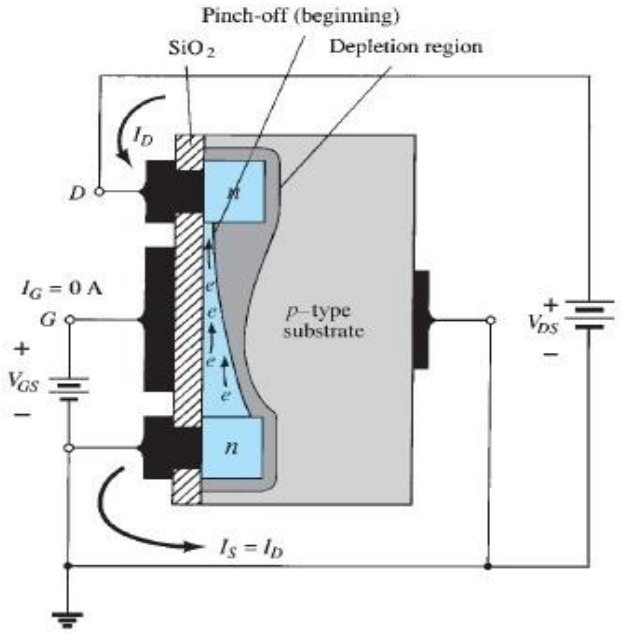
$V_D = V_G + V_T$

$V_D - V_S = V_G - V_S + V_T$

$\mathbf{V_{DS} = V_{GS} + V_T}$ (condition for saturation)

$\mathbf{V_{DS} = V_{GS} + V_{DG}}$

$\mathbf{V_{DG} = V_{DS} - V_{GS}}$ (condition for saturation)

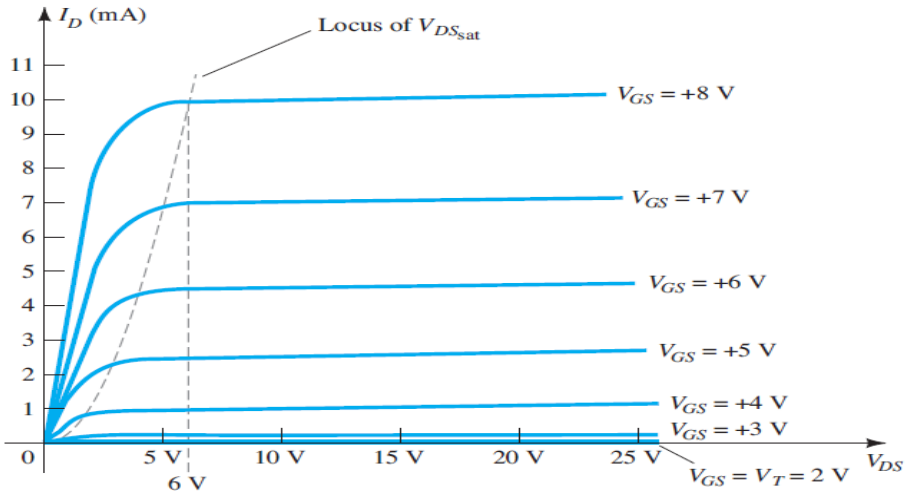



***(Change in channel and depletion region with increasing level of $V_{DS}$ for a fixed value of $V_{GS}$)***

$V_{GS} = 8$ V, saturation occurs at a level of $V_{DS} = 6$ V. In fact, the saturation level for $V_{DS}$ is related to the level of applied $V_{GS}$ by

$$V_{DS_{sat}} = V_{GS} - V_T$$

Obviously, therefore, for a fixed value of $V_T$, the higher the level of $V_{GS}$, the greater is the saturation level for $V_{DS}$, as shown in Fig. by the locus of saturation levels.




*Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V$^2$.*

*For values of $V_{GS}$ less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.*

Figure clearly reveals that as the level of $V_{GS}$ increases from $V_T$ to 8 V, the resulting saturation level for $I_D$ also increases from a level of 0 mA to 10 mA. In addition, it is quite noticeable that the spacing between the levels of $V_{GS}$ increases as the magnitude of $V_{GS}$ increases, resulting in ever-increasing increments in drain current.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Again, it is the squared term that results in the nonlinear (curved) relationship between $I_D$ and $V_{GS}$. The $k$ term is a constant that is a function of the construction of the device. The value of $k$ can be determined from the following equation , where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

Substituting $I_{D(on)} = 10$ mA when $V_{GS(on)} = 8$ V from the characteristics of Fig. yields

$$k = \frac{10 \text{ mA}}{(8 \text{ V} - 2 \text{ V})^2} = \frac{10 \text{ mA}}{(6 \text{ V})^2} = \frac{10 \text{ mA}}{36 \text{ V}^2}$$
$$= \mathbf{0.278 \times 10^{-3} \text{ A/V}^2}$$

and a general equation for $I_D$ for the characteristics of Fig. results in

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2 \text{ V})^2$$

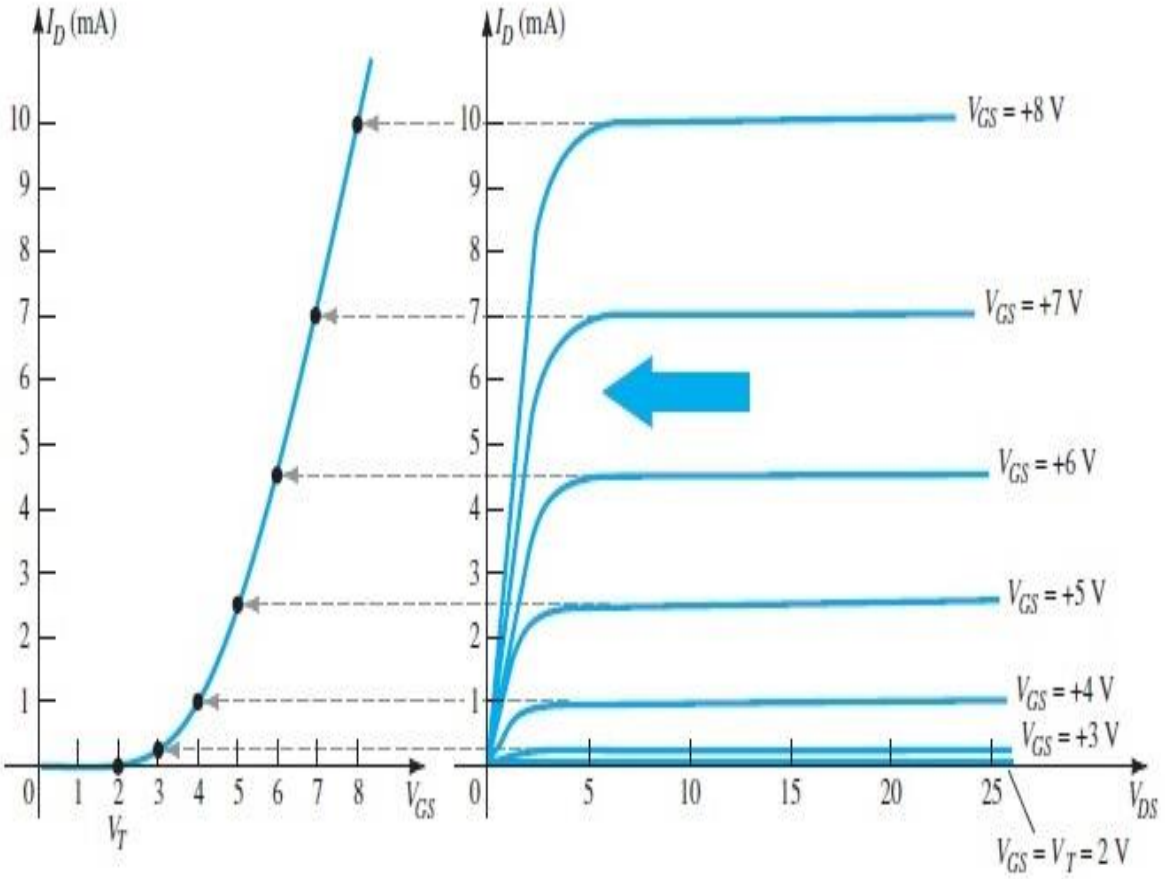
Substituting $V_{GS} = 4$ V, we find that

$$I_D = 0.278 \times 10^{-3}(4 \text{ V} - 2 \text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$
$$= 0.278 \times 10^{-3}(4) = \mathbf{1.11 \text{ mA}}$$

The current voltage relationship is given by the Shockley's equation,

$$\mathbf{I_D = K(V_{GS} - V_T)^2}$$

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed. For values of $V_{GS}$ less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.




***(Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.)***

**problem:-**

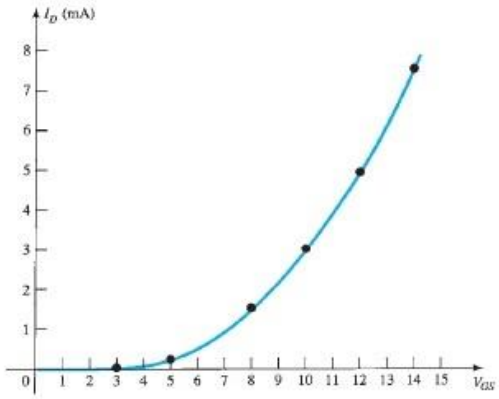
For an E-MOSFET $V_{GS(on)} = 10V$ , $I_{D(on)} = 3mA$ and $V_{Th} = 3V$, determine:
a. The resulting value of *k* for the MOSFET.
b. The transfer characteristics.

**ans:-**

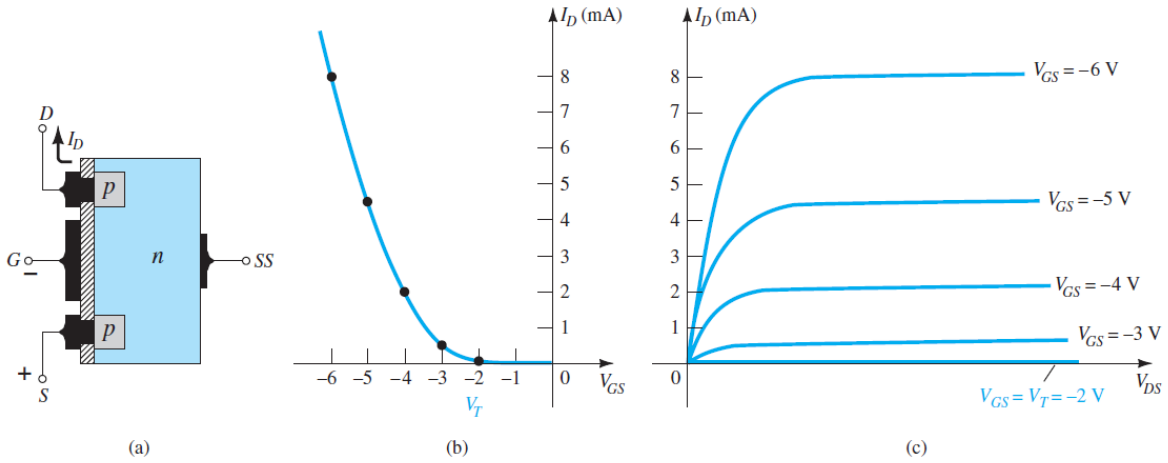
$$I_D = K(V_{GS} - V_{GS(Th)})^2$$
$$I_{D(on)} = K(V_{GS(on)} - V_{GS(Th)})^2$$
$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$
$$K = \frac{3mA}{(10V - 3V)^2}$$

**K= 0.061 mA / $V^2$**

| $V_{GS}$(V) | $I_D$(mA) |
|---|---|
| 3 | 0 |
| 5 | 0.244 |
| 8 | 1.525 |
| 10 | 3 |
| 12 | 4.94 |
| 14 | 7.38 |



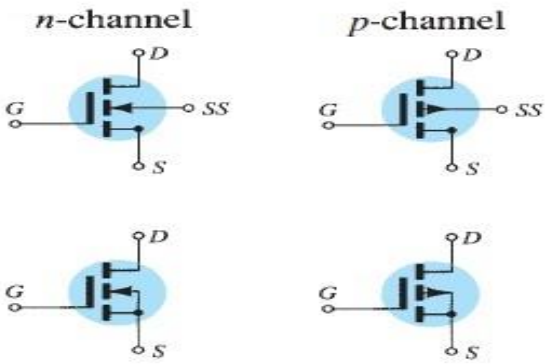

## *p* -Channel Enhancement-Type MOSFETs




*p-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V².*

---

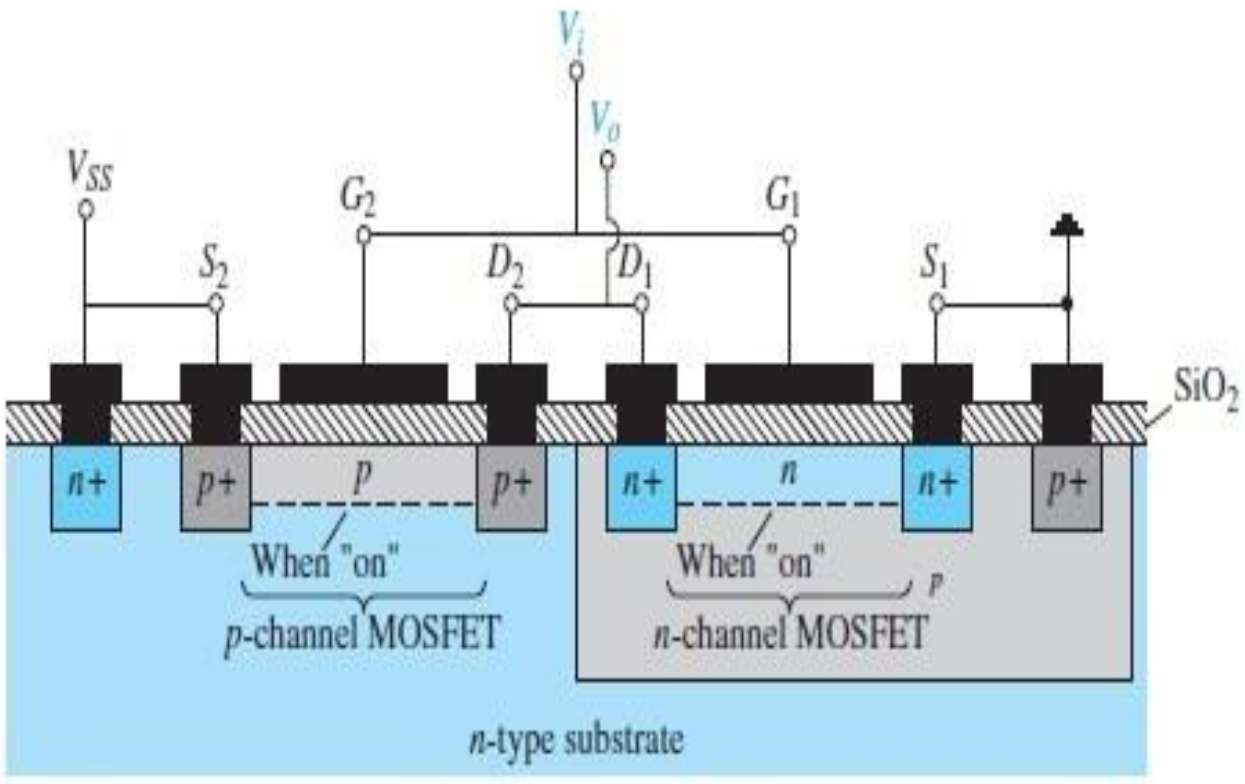
The graphic symbols for the *n* -channel and *p* -channel JFETs are shown below . Note that the arrow is pointing in for the *n* -channel device to represent the direction in which $I_G$ would flow if the *p* – *n* junction was forward-biased. For the *p* -channel device the only difference in the symbol is the direction of the arrow in the symbol.




***(a) n-channel enhancement-type MOSFETs***
***(b) p-channel enhancement type MOSFETs.***

# CMOS

CMOS stands for *complementary MOSFET* which consists of a P-MOS and N-MOS. Here the P-MOS and N-MOS are on the left and right side respectively.



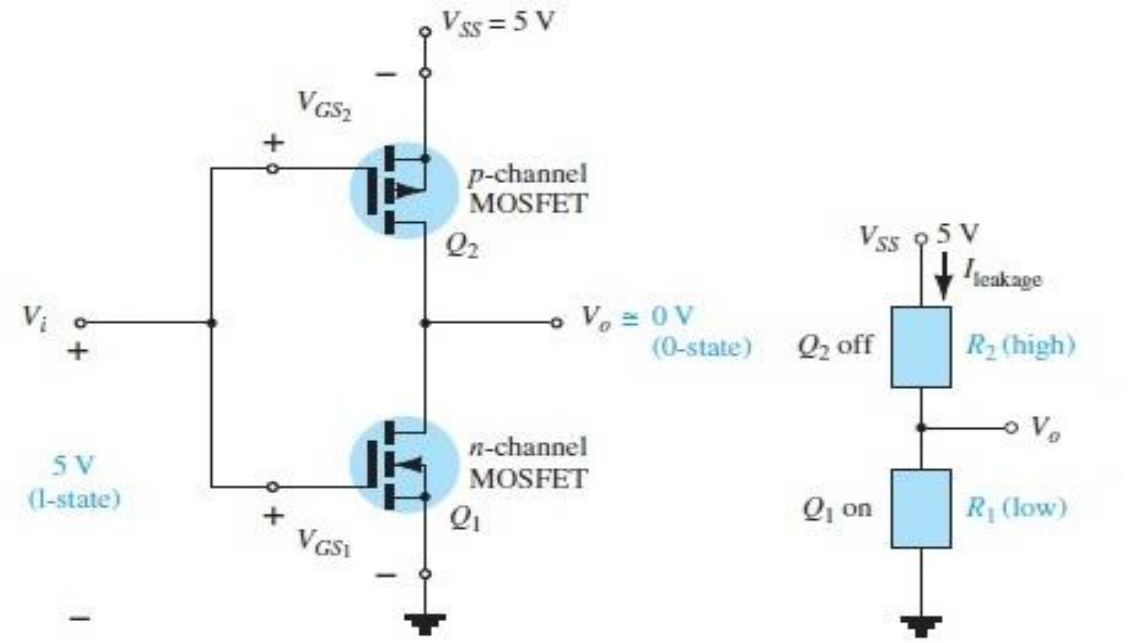

***(Complementary MOSFET* arrangement (CMOS))**

The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as *CMOS logic design.*

**CMOS as INVERTER**

One very effective use of the complementary arrangement is as an inverter, as shown in figure below. As introduced for switching transistors, an inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa.

To design a CMOS inverter both the gates are connected to the applied signal and both drain to the output $V_o$ . The source of the p-channel MOSFET(*Q*2) is connected directly to the applied voltage $V_{SS}$, whereas the source of the n-channel MOSFET(*Q*1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V at the output.




(**CMOS INVERTER**) **(Relative resistance levels for V i = 5 V (1-state))**

With 5 V at $V_i$ (with respect to ground), $V_{GS1} = V_i$ , and Q1 is "on" , resulting in a relatively low resistance between drain and source. Since $V_i$ and $V_{SS}$ are at 5 V, $V_{GS2} = 0$ V, which is less than the required $V_T$ for the device, resulting in an "off" state. The resulting resistance level between drain and source is quite high for Q2.A simple application of the voltage-divider rule will reveal that $V_o$ is very close to 0 V, or the 0-state, establishing the desired inversion process.

For an applied voltage $V_i$ of 0 V (0-state), $V_{GS1} = 0$ V, and Q1 will be "off" with $V_{GS2}$= -5 V, turning on the p-channel MOSFET. The result is that Q2 will present a small resistance level, Q1 a high resistance, and $V_o = VSS = 5$ V (the 1-state). Since the drain current that flows for either case is limited by the "off" transistor to the leakage value, the power dissipated by the device in either state is very low.

# MODULE – 4

## Operational Amplifier

*Operational amplifiers* are linear devices that have all the properties required for nearly ideal DC amplification and are therefore used extensively in signal conditioning, filtering or to perform mathematical operations such as addition, subtraction, integration and differentiation.

An **Operational Amplifier**, or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function or "operation" of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of "Operational Amplifier".

An *Operational Amplifier* is basically a three-terminal device which consists of two high impedance inputs. One of the inputs is called the **Inverting Input**, marked with a negative or "minus" sign, (–). The other input is called the **Non-inverting Input**, marked with a positive or "plus" sign (+).

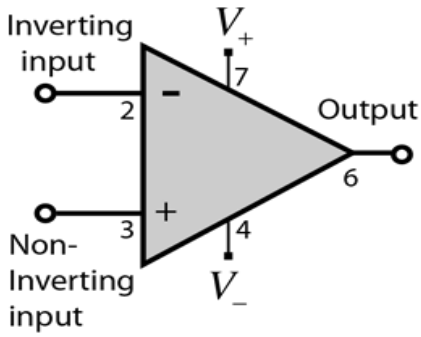


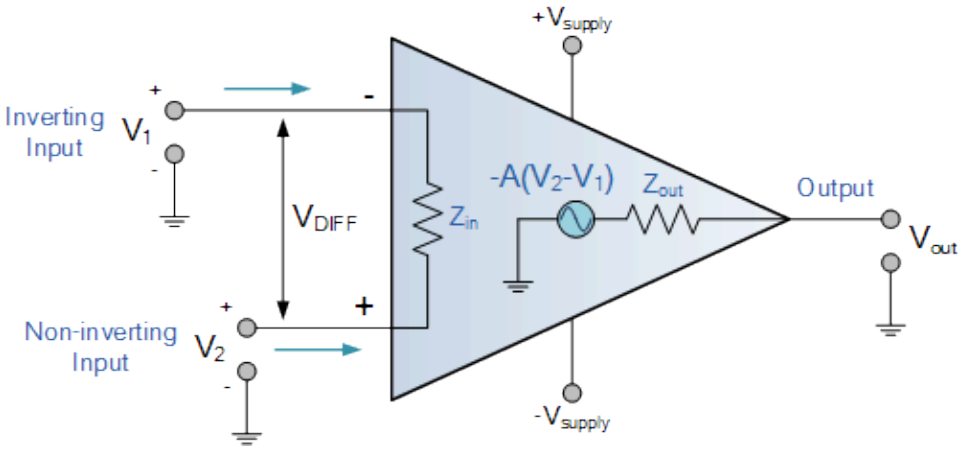

Fig. 4.1 Basic operational amplifier

A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

- Voltage – Voltage "in" and Voltage "out"
- Current – Current "in" and Current "out"
- Transconductance – Voltage "in" and Current "out"

- Transresistance – Current “in” and Voltage “out”

**Equivalent Circuit of an Ideal Operational Amplifier**




**Op-amp Parameter and Idealised Characteristic**

- **Open Loop Gain, ($A_{vo}$)**

  **Infinite** – The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better. Open-loop gain is the gain of the op-amp without positive or negative feedback and for such an amplifier the gain will be infinite but typical real values range from about 20,000 to 200,000.

- **Input impedance, ($Z_{IN}$)**

  **Infinite** – Input impedance is the ratio of input voltage to input current and is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry ( $I_{IN} = 0$ ). Real op-amps have input leakage currents from a few pico-amps to a few milli-amps.

- **Output impedance, ($Z_{OUT}$)**

  **Zero** – The output impedance of the ideal operational amplifier is assumed to be zero acting as a perfect internal voltage source with no internal resistance so that it can supply as much current as necessary to the load. This internal resistance is effectively in series with the load thereby reducing the output voltage available to the load. Real op-amps have output impedances in the 100-20kΩ range.

- **Bandwidth, (BW)**

**Infinite** – An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies so it is therefore assumed to have an infinite bandwidth. With real op-amps, the bandwidth is limited by the Gain-Bandwidth product (GB), which is equal to the frequency where the amplifiers gain becomes unity.

- **Offset Voltage, ($V_{IO}$)**

  **Zero** – The amplifiers output will be zero when the voltage difference between the inverting and the non-inverting inputs is zero, the same or when both inputs are grounded. Real op-amps have some amount of output offset voltage.

From these "idealized" characteristics above, we can see that the input resistance is infinite, so **no current flows into either input terminal** (the "current rule") and that the **differential input offset voltage is zero** (the "voltage rule"). It is important to remember these two properties as they will help us understand the workings of the **Operational Amplifier** with regards to the analysis and design of op-amp circuits.

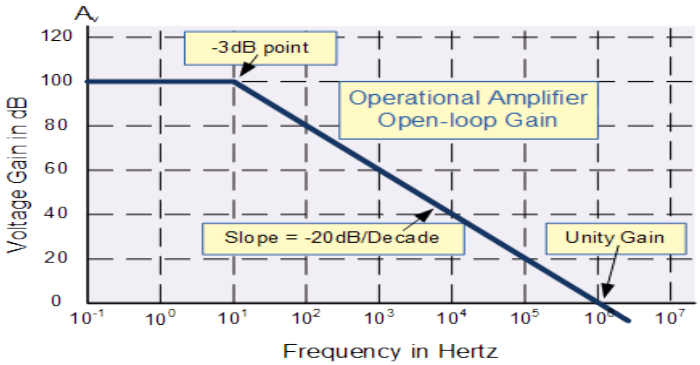
The **Voltage Gain** ($A_V$) of the operational amplifier can be found using the following formula:

$$\text{Voltage Gain, (A)} = \frac{V_{out}}{V_{in}}$$

And in **Decibels** or (dB) is given as:

$$20\log(A) \text{ or } 20\log\frac{V_{out}}{V_{in}} \textit{ in dB}$$

**Open-loop Frequency Response Curve**




From this frequency response curve we can see that the product of the gain against frequency is constant at any point along the curve. Also that the unity gain (0dB) frequency

also determines the gain of the amplifier at any point along the curve. This constant is generally known as the **Gain Bandwidth Product** or **GBP**. Therefore:

GBP = Gain x Bandwidth = A x BW

For example, from the graph above the gain of the amplifier at 100kHz is given as 20dB or 10, then the gain bandwidth product is calculated as:

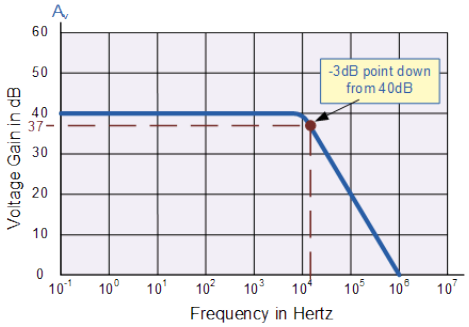
GBP = A x BW = 10 x 100,000Hz = 1,000,000.

Similarly, the operational amplifiers gain at 1kHz = 60dB or 1000, therefore the GBP is given as:

GBP = A x BW = 1,000 x 1,000Hz = 1,000,000. **The same!**.

**An Operational Amplifiers Bandwidth**

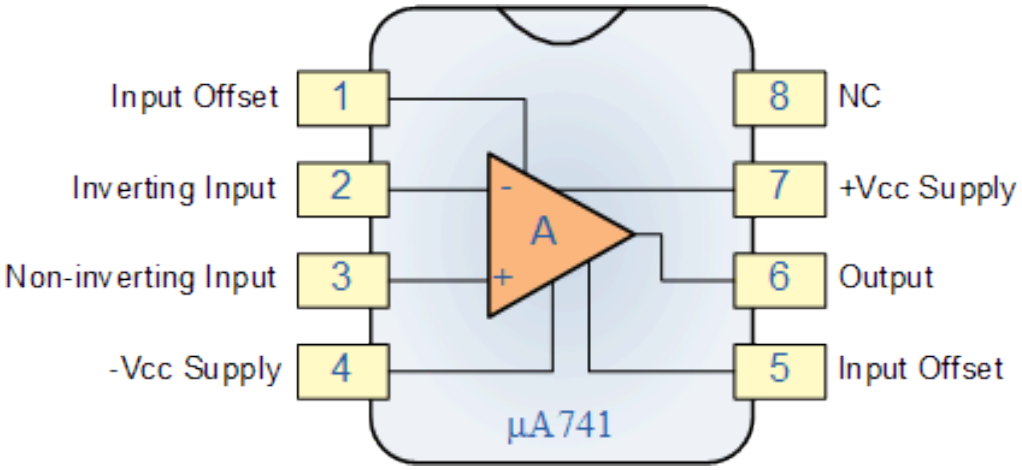
The operational amplifiers bandwidth is the frequency range over which the voltage gain of the amplifier is above **70.7%** or **-3dB** (where 0dB is the maximum) of its maximum output value as shown below.




Here we have used the 40dB line as an example. The -3dB or 70.7% of Vmax down point from the frequency response curve is given as **37dB**. Taking a line across until it intersects with the main GBP curve gives us a frequency point just above the 10kHz line at about 12 to 15kHz. We can now calculate this more accurately as we already know the GBP of the amplifier, in this particular case 1MHz.

There are a very large number of operational amplifier IC's available to suit every possible application from standard bipolar, precision, high-speed, low-noise, high-voltage, etc, in either standard configuration or with internal Junction FET transistors.

Operational amplifiers are available in IC packages of either single, dual or quad op-amps within one single device. The most commonly available and used of all operational amplifiers in basic electronic kits and projects is the industry standard **µA-741**.




## Ideal Op-Amp Characteristics

An ideal op-amp should have the following characteristics:

1. Infinite voltage gain (So that maximum output is obtained)
2. Infinite input resistance (Due to this almost any source can drive it)
3. Zero output resistance (So that there is no change in output due to change in load current)
4. Infinite bandwidth
5. Zero noise
6. Zero power supply rejection ratio (PSSR = 0)
7. Infinite common mode rejection ratio (CMMR = ∞)

**Practical Operational Amplifier**

None of the above-given parameters can be practically realized. A practical or real op-amp has some unavoidable imperfections and hence its characteristics differ from the ideal one. A real op-amp will have non-zero and non-infinite parameters.

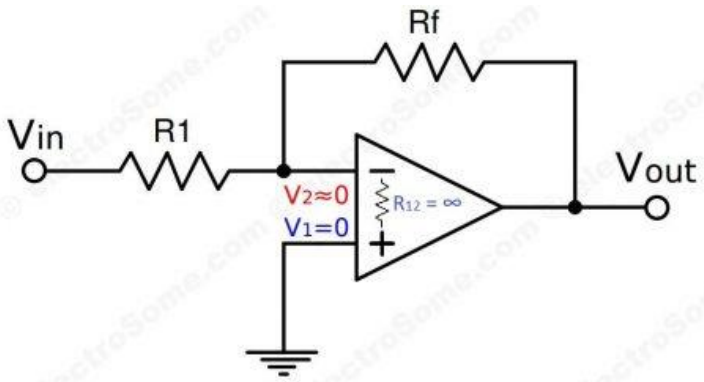
**Virtual Ground**

A **virtual ground** is a result of an op-amp trying to keep its two input terminals at the same potential when used **in a** feedback circuit. **Real ground** is when a terminal is connected physically to the **ground** or earthed to complete the circuit with phase.

As the name indicates it is virtual, not real ground. For some purposes we can consider it as equivalent to ground. In op-amps **the term virtual ground means that the voltage at that particular node is almost equal to ground voltage** (0V). It is **not** physically connected to ground. This concept is very useful in analysis of op-amp circuits and it will make a lot of calculations very simple.

In electronics, '**short**' between two points (or **short** circuit) is referred as those two points are at same potential or they are shorted (connected) by a simple wire. By **virtual short** concept, we can say voltage at inverting terminal (v-) tracks the voltage at non-inverting terminal (v+) under NEGATIVE feedback.

**Virtual Ground in Op-amp**




We already know that an ideal op-amp will provide infinite voltage gain. For real op-amps also the gain will be very high such that we can consider it as infinite for calculation purposes.

- **Gain = $V_o/V_{in}$**

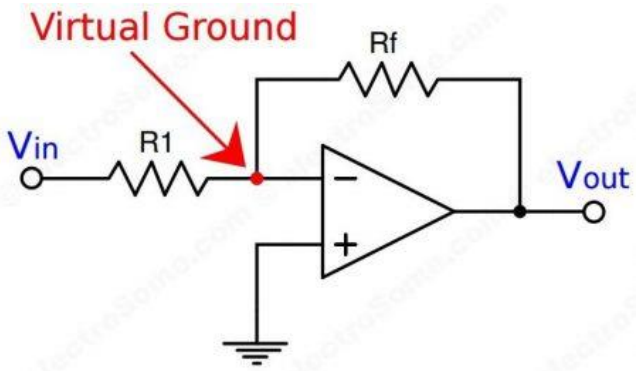
As gain is infinite, **$V_{in} = 0$**

- $V_{in} = V_2 - V_1$

In the above circuit $V_1$ is connected to ground, so $V_1 = 0$. Thus $V_2$ also will be at ground potential.

- **$V_2 = 0$**

Virtual Ground concept is very useful in analysis of an op-amp when negative feedback is employed. It will simply a lot of calculations and derivations.



**Applications of Operational Amplifier**

The integrated op-amps offer all the advantages of ICs such as high reliability, small size, cheap, less power consumption. They are used in variety of applications such as inverting amplifier and non-inverting amplifiers, unity gain buffer, summing amplifier, differentiator, integrator, adder, instrumentation amplifier, Wien bridge oscillator, Filters etc.

**APPLICATIONS OF OP-AMP**

**1. Inverting Operational Amplifier**

In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal" and that "V1 always equals V2". However, in real world op-amp circuits both of these rules are slightly broken.

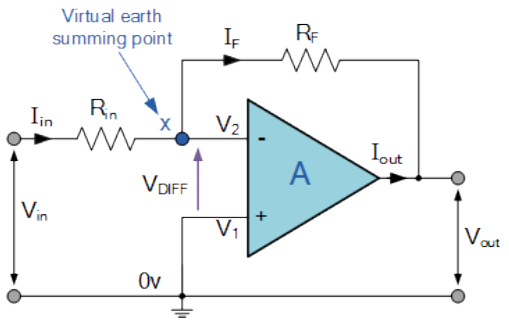



Fig. 4.2 Inverting Operational Amplifier

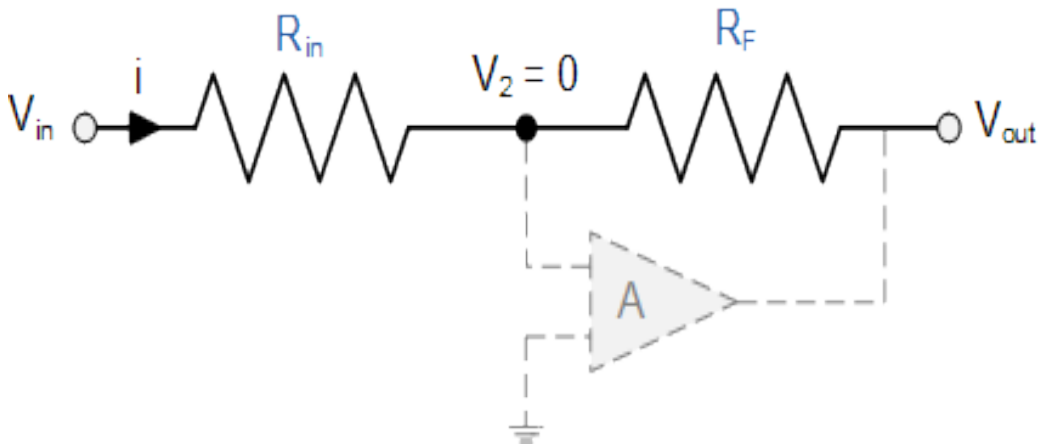
This is because the junction of the input and feedback signal (X) is at the same potential as the positive ( + ) input which is at zero volts or ground then, the junction is a **"Virtual Ground"**. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, $R_{in}$ and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

We said above that there are two very important rules to remember about **Inverting Amplifiers** or any operational amplifier for that matter and these are.

- No Current Flows into the Input Terminals
- The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)

Then by using these two rules we can derive the equation for calculating the closed-loop gain of an inverting amplifier, using first principles.

Current (i) flows through the resistor network as shown.




$$i = \frac{Vin - Vout}{Rin + Rf}$$

$$\text{therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$$

$$i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$$

$$\text{so, } \frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$$

$$\text{and as, } i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf} \qquad \frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$$

$$\text{the Closed Loop Gain (Av) is given as, } \frac{Vout}{Vin} = -\frac{Rf}{Rin}$$

Then, the **Closed-Loop Voltage Gain** of an Inverting Amplifier is given as.

$$\text{Gain (Av)} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

And this can be transposed to give $V_{out}$ as:

$$Vout = -\frac{Rf}{Rin} \times Vin$$

The negative sign in the equation indicates an inversion of the output signal with respect to the input as it is 180° out of phase. This is due to the feedback being negative in value. The equation for the output voltage Vout also shows that the circuit is linear in nature for a fixed amplifier gain as $V_{out} = V_{in}$ x Gain. This property can be very useful for converting a smaller sensor signal to a much larger voltage.

**2. Non-inverting Operational Amplifier**

In this configuration, the input voltage signal, ( $V_{IN}$ ) is applied directly to the non-inverting ( + ) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit we saw in the last tutorial whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.

Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting (–) input terminal via a $R_f - R_2$ voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, a very high input impedance, Rin approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and a low output impedance, Rout as shown below.

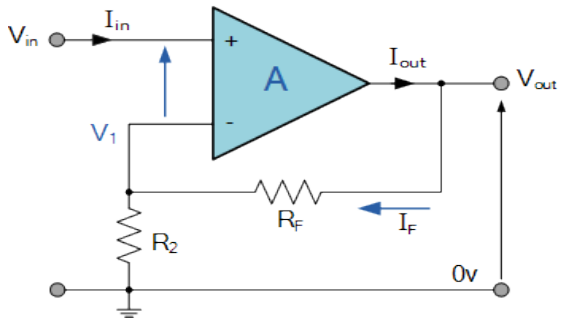
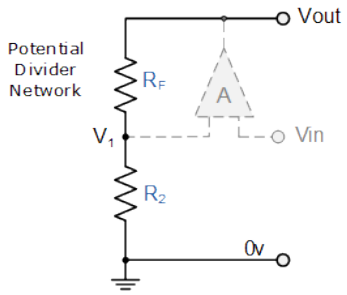



Fig. 4.3 Non-inverting Operational Amplifier Configuration

In the previous Inverting Amplifier tutorial, we said that for an ideal op-amp "No current flows into the input terminal" of the amplifier and that "$V_1$ always equals $V_2$". This was because the junction of the input and feedback signal ($V_1$) are at the same potential.

In other words the junction is a "virtual earth" summing point. Because of this virtual earth node the resistors, $R_f$ and $R_2$ form a simple potential divider network across the non-inverting amplifier with the voltage gain of the circuit being determined by the ratios of $R_2$ and $R_f$ as shown below.

**Equivalent Potential Divider Network**




Then using the formula to calculate the output voltage of a potential divider network, we can calculate the closed-loop voltage gain ($A_V$) of the **Non-inverting Amplifier** as follows:

$$V_1 = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

$$\text{Ideal Summing Point: } V_1 = V_{IN}$$

$$\text{Voltage Gain, } A_{(V)} \text{ is equal to: } \frac{V_{OUT}}{V_{IN}}$$

$$\text{Then, } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$$

$$\text{Transpose to give: } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$$

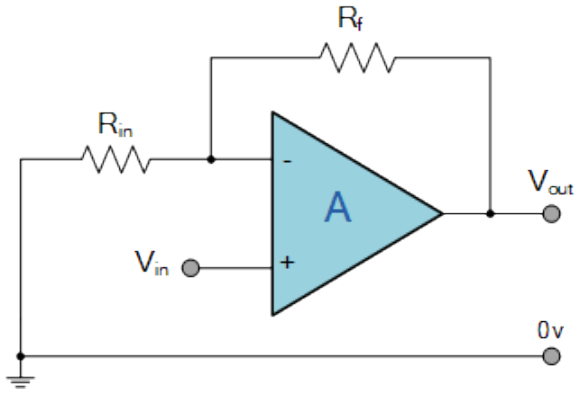
Then the closed loop voltage gain of a **Non-inverting Operational Amplifier** will be given as:

$$A_{(v)} = 1 + \frac{R_F}{R_2}$$

We can see from the equation above that the overall closed-loop gain of a non-inverting amplifier will always be greater but never less than one (unity), it is positive in nature and is determined by the ratio of the values of $R_f$ and $R_2$.

If the value of the feedback resistor $R_f$ is zero, the gain of the amplifier will be exactly equal to one (unity). If resistor $R_2$ is zero the gain will approach infinity, but in practice it will be limited to the operational amplifiers open-loop differential gain, ($A_O$).

We can easily convert an inverting operational amplifier configuration into a non-inverting amplifier configuration by simply changing the input connections as shown.




**3. Voltage Follower (Unity Gain Buffer)**

If we made the feedback resistor, $R_f$ equal to zero, ($R_f = 0$), and resistor $R_2$ equal to infinity, ($R_2 = \infty$), then the circuit would have a fixed gain of "1" as all the output voltage would be present on the inverting input terminal (negative feedback). This would then produce a special type of the non-inverting amplifier circuit called a **Voltage Follower** or also called a "unity gain buffer".

As the input signal is connected directly to the non-inverting input of the amplifier the output signal is not inverted resulting in the output voltage being equal to the input voltage, $V_{out} = V_{in}$. This then makes the **voltage follower** circuit ideal as a Unity Gain Buffer circuit because of its isolation properties.

The advantage of the unity gain voltage follower is that it can be used when impedance matching or circuit isolation is more important than amplification as it maintains the signal voltage. The input impedance of the voltage follower circuit is very high, typically above 1MΩ as it is equal to that of the operational amplifiers input resistance times its gain ( $R_{in}$ x $A_O$ ). Also its output impedance is very low since an ideal op-amp condition is assumed.

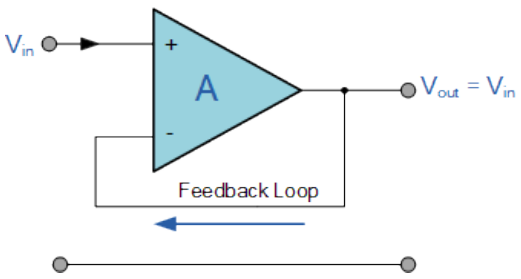



Fig. 4.4 Non-inverting Voltage Follower

In this non-inverting circuit configuration, the input impedance $R_{in}$ has increased to infinity and the feedback impedance $R_f$ reduced to zero. The output is connected directly back to the negative inverting input so the feedback is 100% and $V_{in}$ is exactly equal to Vout giving it a fixed gain of 1 or unity. As the input voltage $V_{in}$ is applied to the non-inverting input the gain of the amplifier is given as:

$$V_{out} = A(V_{in})$$

$$(V_{in} = V+) \text{ and } (V_{out} = V-)$$

$$\text{therefore Gain, } (A_V) = \frac{V_{out}}{V_{in}} = +1$$

Since no current flows into the non-inverting input terminal the input impedance is infinite (ideal op-amp) and also no current flows through the feedback loop so any value of resistance may be placed in the feedback loop without affecting the characteristics of the circuit as no voltage is dissipated across it, zero current flows, zero voltage drop, zero power loss.

As the input current is zero giving zero input power, the voltage follower can provide a large power gain. However in most real unity gain buffer circuits a low value (typically 1kΩ) resistor is required to reduce any offset input leakage currents, and also if the operational amplifier is of a current feedback type.

The voltage follower or unity gain buffer is a special and very useful type of **Non-inverting amplifier** circuit that is commonly used in electronics to isolated circuits from each other especially in High-order state variable or Sallen-Key type active filters to separate one filter stage from the other.

One final thought, the closed loop voltage gain of a voltage follower circuit is "1" or **Unity**. The open loop voltage gain of an operational amplifier with no feedback is **Infinite**. Then by carefully selecting the feedback components we can control the amount of gain produced by a non-inverting operational amplifier anywhere from one to infinity.

Thus far we have analysed an inverting and non-inverting amplifier circuit that has just one input signal, $V_{in}$. In the next tutorial about Operational Amplifiers, we will examine the effect of the output voltage, Vout by connecting more inputs to the amplifier. This then produces another common type of operational amplifier circuit called a Summing Amplifier which can be used to "add" together the voltages present on its inputs.

## 4. The Summing Amplifier

The **Summing Amplifier** is another type of operational amplifier circuit configuration that is used to combine the voltages present on two or more inputs into a single output voltage.

### (a) Inverting Summing Amplifier

We saw previously in the inverting operational amplifier that the inverting amplifier has a single input voltage, ($V_{in}$) applied to the inverting input terminal. If we add more input resistors to the input, each equal in value to the original input resistor, ($R_{in}$) we end up with another operational amplifier circuit called a **Summing Amplifier**, "*summing inverter*" or even a "*voltage adder*" circuit as shown below.

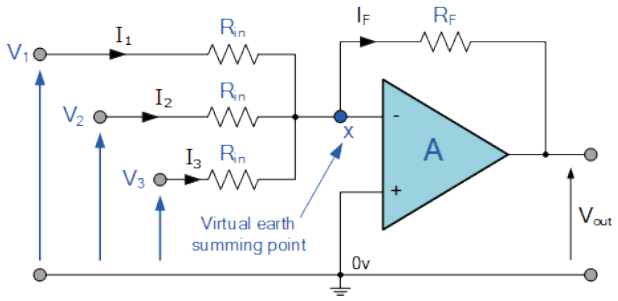



Fig. 4.5 Inverting Summing Amplifier Circuit

In this simple summing amplifier circuit, the output voltage, ($V_{out}$) now becomes proportional to the sum of the input voltages, $V_1$, $V_2$, $V_3$, etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$

However, if all the input impedances, ($R_{IN}$) are equal in value, we can simplify the above equation to give an output voltage of:

Summing Amplifier Equation

$$-Vout = \frac{R_F}{R_{IN}}\left(V1 + V2 + V3 \ldots . etc\right)$$

We now have an operational amplifier circuit that will amplify each individual input voltage and produce an output voltage signal that is proportional to the algebraic "SUM" of the three individual input voltages $V_1$, $V_2$ and $V_3$. We can also add more inputs if required as each individual input "see's" their respective resistance, $R_{in}$ as the only input impedance.

This is because the input signals are effectively isolated from each other by the "virtual earth" node at the inverting input of the op-amp. A direct voltage addition can also be obtained when all the resistances are of equal value and $R_f$ is equal to $R_{in}$.

Note that when the summing point is connected to the inverting input of the op-amp the circuit will produce the negative sum of any number of input voltages. Likewise, when the summing point is connected to the non-inverting input of the op-amp, it will produce the positive sum of the input voltages.

A **Scaling Summing Amplifier** can be made if the individual input resistors are "NOT" equal. Then the equation would have to be modified to:

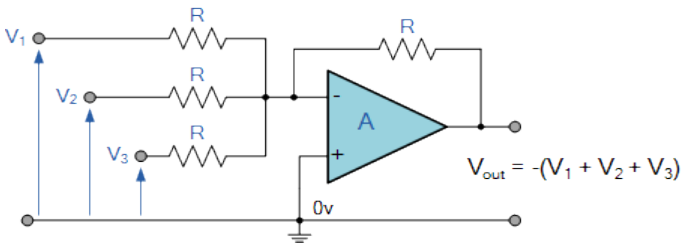
$$-V_{OUT} = V_1\left(\frac{R_f}{R_1}\right) + V_2\left(\frac{R_f}{R_2}\right) + V_3\left(\frac{R_f}{R_3}\right) \ldots . etc$$

To make the math's a little easier, we can rearrange the above formula to make the feedback resistor $R_f$ the subject of the equation giving the output voltage as:

$$-V_{OUT} = R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) \ldots . etc$$

This allows the output voltage to be easily calculated if more input resistors are connected to the amplifiers inverting input terminal. The input impedance of each individual channel is the value of their respective input resistors, i.e., $R_1$, $R_2$, $R_3$ … etc.

Sometimes we need a summing circuit to just add together two or more voltage signals without any amplification. By putting all of the resistances of the circuit above to the same value R, the op-amp will have a voltage gain of unity and an output voltage equal to the direct sum of all the input voltages as shown:




The **Summing Amplifier** is a very flexible circuit indeed, enabling us to effectively "Add" or "Sum" (hence its name) together several individual input signals. If the inputs resistors, $R_1$, $R_2$, $R_3$ etc, are all equal a "unity gain inverting adder" will be made. However, if the input resistors are of different values a "scaling summing amplifier" is produced which will output a weighted sum of the input signals.

**(b) Non-inverting Summing Amplifier**

But as well as constructing inverting summing amplifiers, we can also use the non-inverting input of the operational amplifier to produce a *non-inverting summing amplifier*. We have seen above that an inverting summing amplifier produces the negative sum of its input voltages then it follows that the non-inverting summing amplifier configuration will produce the positive sum of its input voltages.

As its name implies, the non-inverting summing amplifier is based around the configuration of a non-inverting operational amplifier circuit in that the input (either ac or dc) is applied to the non-inverting (+) terminal, while the required negative feedback and gain is achieved by feeding back some portion of the output signal ($V_{OUT}$) to the inverting (-) terminal as shown.

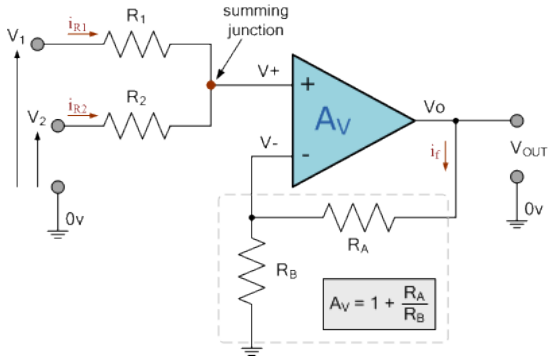



Fig. 4.6 Non-inverting Summing Amplifier

So, what's the advantage of the non-inverting configuration compared to the inverting summing amplifier configuration. Besides the most obvious fact that the op-amps output voltage $V_{OUT}$ is in phase with its input, and the output voltage is the weighted sum of all its inputs which themselves are determined by their resistance ratios, the biggest advantage of the non-inverting summing amplifier is that because there is no virtual earth condition across the input terminals, its input impedance is much higher than that of the standard inverting amplifier configuration.

Also, the input summing part of the circuit is unaffected if the op-amps closed-loop voltage gain is changed. However, there is more maths involved in selecting the weighted gains for each individual input at the summing junction especially if there are more than two inputs each with a different weighting factor. Nevertheless, if all the inputs have the same resistive values, then the maths involved will be a lot less.

If the closed-loop gain of the non-inverting operational amplifier is made equal the number of summing inputs, then the op-amps output voltage will be exactly equal to the sum of all the input voltages. That is for a two input non-inverting summing amplifier, the op-amps gain is equal to 2, for a three-input summing amplifier the op-amps gain is 3, and so on. This is because the currents which flow in each input resistor is a function of the voltage at all its inputs. If the input resistances made all equal, ($R_1 = R_2$) then the circulating currents cancel out as they cannot flow into the high impedance non-inverting input of the op-amp and the $v_{output}$ voltage becomes the sum of its inputs.

So, for a 2-input non-inverting summing amplifier the currents flowing into the input terminals can be defined as:

$$I_{R1} + I_{R2} = 0 \quad (\text{KCL})$$

$$\frac{V_1 - V+}{R_1} = \frac{V_2 - V+}{R_2} = 0$$

$$\therefore \left(\frac{V_1}{R_1} - \frac{V+}{R_1}\right) + \left(\frac{V_2}{R_2} - \frac{V+}{R_2}\right) = 0$$

If we make the two input resistances equal in value, then $R_1 = R_2 = R$.

$$V+ = \frac{\frac{V_1}{R} + \frac{V_2}{R}}{\frac{1}{R} + \frac{1}{R}} = \frac{\frac{V_1 + V_2}{R}}{\frac{2}{R}}$$

$$\text{Thus} \quad V+ = \frac{V_1 + V_2}{2}$$

The standard equation for the voltage gain of a non-inverting summing amplifier circuit is given as:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{V_{OUT}}{V+} = 1+\frac{R_A}{R_B}$$

$$\therefore \; V_{OUT} = \left[1 + \frac{R_A}{R_B}\right] V+$$

$$\text{Thus:} \quad V_{OUT} = \left[1 + \frac{R_A}{R_B}\right] \frac{V_1 + V_2}{2}$$

The non-inverting amplifiers closed-loop voltage gain $A_V$ is given as: $1 + R_A/R_B$. If we make this closed-loop voltage gain equal to 2 by making $R_A = R_B$, then the output voltage $V_O$ becomes equal to the sum of all the input voltages as shown.

Non-inverting Summing Amplifier Output Voltage

$$V_{OUT} = \left[1 + \frac{R_A}{R_B}\right] \frac{V_1 + V_2}{2}$$

$$\text{If} \;\; R_A = R_B$$

$$V_{OUT} = [1+1] \frac{V_1 + V_2}{2} = 2 \frac{V_1 + V_2}{2}$$

$$\therefore V_{OUT} = V_1 + V_2$$

Thus, for a 3-input non-inverting summing amplifier configuration, setting the closed-loop voltage gain to 3 will make $V_{OUT}$ equal to the sum of the three input voltages, $V_1$, $V_2$ and $V_3$. Likewise, for a four-input summer, the closed-loop voltage gain would be 4, and 5 for a 5-input summer, and so on. Note also that if the amplifier of the summing circuit is connected as a unity follower with $R_A$ equal to zero and $R_B$ equal to infinity, then with no voltage gain the output voltage $V_{OUT}$ will be exactly equal the average value of all the input voltages. That is $V_{OUT} = (V_1 + V_2)/2$.

## 6. The Differential Amplifier

The differential amplifier amplifies the voltage difference present on its inverting and non-inverting inputs

Thus far we have used only one of the operational amplifiers inputs to connect to the amplifier, using either the “inverting” or the “non-inverting” input terminal to amplify a single input signal with the other input being connected to ground.

But as a standard operational amplifier has two inputs, inverting and no-inverting, we can also connect signals to both of these inputs at the same time producing another common type of operational amplifier circuit called a **Differential Amplifier**.

Basically, as we saw in the first tutorial about operational amplifiers, all op-amps are "Differential Amplifiers" due to their input configuration. But by connecting one voltage signal onto one input terminal and another voltage signal onto the other input terminal the resultant output voltage will be proportional to the "Difference" between the two input voltage signals of $V_1$ and $V_2$.

Then *differential amplifiers* amplify the difference between two voltages making this type of operational amplifier circuit a **Subtractor** unlike a summing amplifier which adds or sums together the input voltages. This type of operational amplifier circuit is commonly known as a **Differential Amplifier** configuration and is shown below:

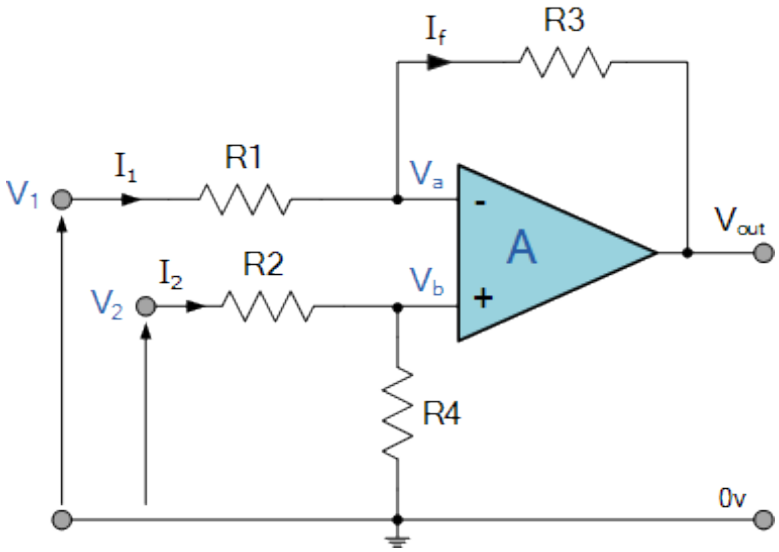



Fig. 4.7 Differential Amplifier Circuit

By connecting each input in turn to 0v ground we can use superposition to solve for the output voltage Vout. Then the transfer function for a **Differential Amplifier** circuit is given as:

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_f = \frac{V_a - (V_{out})}{R_3}$$

$$\text{Summing point } V_a = V_b$$

$$\text{and } V_b = V_2\left(\frac{R_4}{R_2 + R_4}\right)$$

$$\text{If } V_2 = 0, \text{ then: } V_{out(a)} = -V_1\left(\frac{R_3}{R_1}\right)$$

$$\text{If } V_1 = 0, \text{ then: } V_{out(b)} = V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

$$V_{out} = -V_{out(a)} + V_{out(b)}$$

$$\therefore V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

When resistors, R1 = R2 and R3 = R4 the above transfer function for the differential amplifier can be simplified to the following expression:

Differential Amplifier Equation

$$V_{OUT} = \frac{R_3}{R_1}\left(V_2 - V_1\right)$$

If all the resistors are all of the same ohmic value, that is: R1 = R2 = R3 = R4 then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be Vout = $V_2 - V_1$.

Also note that if input $V_1$ is higher than input $V_2$ the output voltage sum will be negative, and if $V_2$ is higher than $V_1$, the output voltage sum will be positive.

The **Differential Amplifier** circuit is a very useful op-amp circuit and by adding more resistors in parallel with the input resistors $R_1$ and $R_3$, the resultant circuit can be made to either "Add" or "Subtract" the voltages applied to their respective inputs.

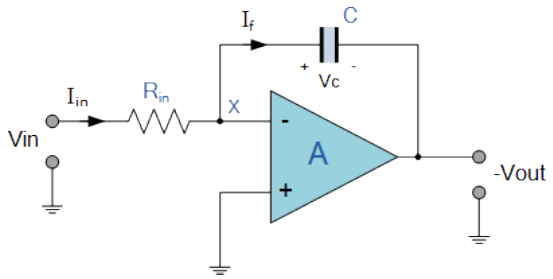
## 7. The Integrator

The integrator Op-amp produces an output voltage that is both proportional to the amplitude and duration of the input signal.

Operational amplifiers can be used as part of a positive or negative feedback amplifier or as an adder or subtractor type circuit using just pure resistances in both the input and the feedback loop.

But what if we were to change the purely resistive ( $R_f$ ) feedback element of an inverting amplifier to that of a frequency dependant reactance, ( X ) type complex element, such as a Capacitor, C. What would be the effect on the op-amps output voltage over its frequency range.

By replacing this feedback resistance with a capacitor, we now have an RC Network connected across the operational amplifiers feedback path producing another type of operational amplifier circuit commonly called an **Op-amp Integrator** circuit as shown below.




(Op-amp Integrator Circuit)

As its name implies, the **Op-amp Integrator** is an operational amplifier circuit that performs the mathematical operation of **Integration** that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces an *output voltage which is proportional to the integral of the input voltage*.

In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

When a step voltage, $V_{in}$ is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit allowing maximum current to flow via the input resistor, $R_{in}$ as potential difference exists between the two plates. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the impedance of the capacitor at this point is very low, the gain ratio of $X_C/R_{IN}$ is also very small giving an overall voltage gain of less than one, (voltage follower circuit).

As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance $X_c$ slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, (τ) of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp's inverting input.

Since the capacitor is connected between the op-amp's inverting input (which is at earth potential) and the op-amp's output (which is negative), the potential voltage, $V_c$ developed across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of $X_c/R_{in}$ increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

At this point the capacitor acts as an open circuit, blocking any more flow of DC current. The ratio of feedback capacitor to input resistor ($X_C/R_{IN}$) is now infinite resulting in infinite gain. The result of this high gain (similar to the op-amps open-loop gain), is that the output of the amplifier goes into saturation as shown below. (Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between).

We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving Q/C. Then the voltage across the capacitor is output $V_{out}$ therefore: $-V_{out} = Q/C$. If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as:

$$V_c = \frac{Q}{C}, \qquad V_c = V_x - V_{out} = 0 - V_{out}$$

$$\therefore \; -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C}\frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, X = 0, the input current I(in) flowing through the input resistor, $R_{in}$ is given as:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

The current flowing through the feedback capacitor C is given as:

$$I_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out}.C}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out}.C}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 1$$

From which we derive an ideal voltage output for the **Op-amp Integrator** as:

$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$$

To simplify the math's a little, this can also be re-written as:

$$V_{out} = -\frac{1}{j\omega RC}V_{in}$$

Where: $\omega = 2\pi f$ and the output voltage $V_{out}$ is a constant 1/RC times the integral of the input voltage $V_{in}$ with respect to time. The minus sign (–) indicates a 180° phase shift because the input signal is connected directly to the inverting input terminal of the op-amp.

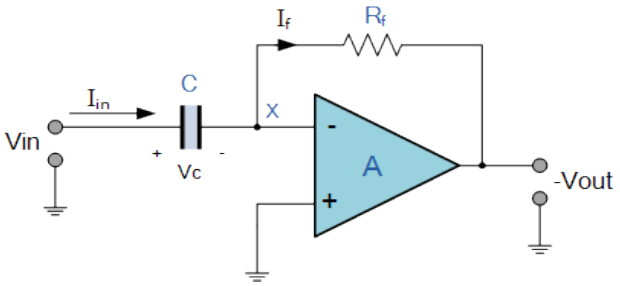
## 8. The Differentiator

The basic operational amplifier differentiator circuit produces an output signal which is the first derivative of the input signal

Here, the position of the capacitor and resistor have been reversed and now the reactance, $X_C$ is connected to the input terminal of the inverting amplifier while the resistor, $R_f$ forms the negative feedback element across the operational amplifier as normal.

This operational amplifier circuit performs the mathematical operation of **Differentiation** that is it "*produces a voltage output which is directly proportional to the input voltage's rate-of-change with respect to time*". In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a "spike" in shape.

As with the integrator circuit, we have a resistor and capacitor forming an RC Network across the operational amplifier and the reactance ($X_c$) of the capacitor plays a major role in the performance of a **Op-amp Differentiator**.




Op-amp Differentiator Circuit

The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain ( $R_f/X_c$ ) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor $R_f$.

Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \text{ and } I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance times Voltage across the capacitor

$$Q = C \times V_{IN}$$

Thus the rate of change of this charge is:

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current, *i*

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

From which we have an ideal voltage output for the op-amp differentiator is given as:

$$V_{OUT} = -R_F C\frac{dV_{IN}}{dt}$$

Therefore, the output voltage $V_{out}$ is a constant $-R_f*C$ times the derivative of the input voltage $V_{in}$ with respect to time. The minus sign (–) indicates a 180° phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

One final point to mention, the **Op-amp Differentiator** circuit in its basic form has two main disadvantages compared to the previous operational amplifier integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed-loop stability is required.

## Common Mode Rejection Ratio (CMRR) of Operational Amplifier

The CMRR (Common Mode Rejection Ratio) is the most important specification and it indicates the how much of the common mode signals will present to measure. The value of the CMMR frequently depends on the signal frequency and the function should be specified. The function of the CMMR is specifically used to reduce the noise on the transmission lines. For an example, when we measure the resistance of a thermocouple in the noisy environment the noise from the environment appears as an offset on both input leads and making it as a common mode voltage signal. The CMRR instrument determines the attenuation applied to the noise.

The CMRR in an operational amplifier is a common mode rejection ratio. Generally, the op amp as two input terminals which are positive and negative terminals and the two inputs are applied at the same point. This will give the opposite polarity signals at the output. Hence the positive and the negative voltage of the terminals will cancel out and it will give the resultant output voltage. The ideal op amp will have the infinite CMRR and with the finite differential gain and zero common mode gain.

**CMMR = Differential mode gain / Common-mode gain**

The common mode rejection ratio is formed by the two inputs which will have the same sign of DC voltage. If we assume one input voltage is 8v and the other 9v here the 8v is common and the input voltage should be calculated through the equation of V+ – V- . Hence the result will be 1v but the common DC voltage between the two inputs has a non-zero gain.

The differential gain Ad magnifies the difference between the two input voltages. But the common mode gain Ac magnifies the common mode DC voltage between the two inputs. The ratio of two gains is said to be as a common mode rejection ratio. The value of the format is in dB. The formula of a common mode rejection ratio is calculated by the following equation.

$$\mathbf{CMRR = 20log|A_d/A_c|\ dB}$$

Where, $A_d$ = Differential gain
and $A_c$ = Common mode gain

**Slew Rate of OP-amp**

The **slew rate** of an **op amp** or any amplifier circuit is the **rate** of change in the output voltage caused by a step change on the input. It is measured as a voltage change in a given time - typically V / µs or V / ms. A typical general purpose device may have a **slew rate** of 10 V / microsecond.

The slew rate of an electronic circuit is defined as the rate of change of the voltage per unit time. Slew rate is usually expressed in units of V/µs.

$$SR=\max\left|\frac{dv_{out}(t)}{dt}\right|$$

Where $v_{out}(t)$ is the output produced by the amplifier as a function of time $t$.

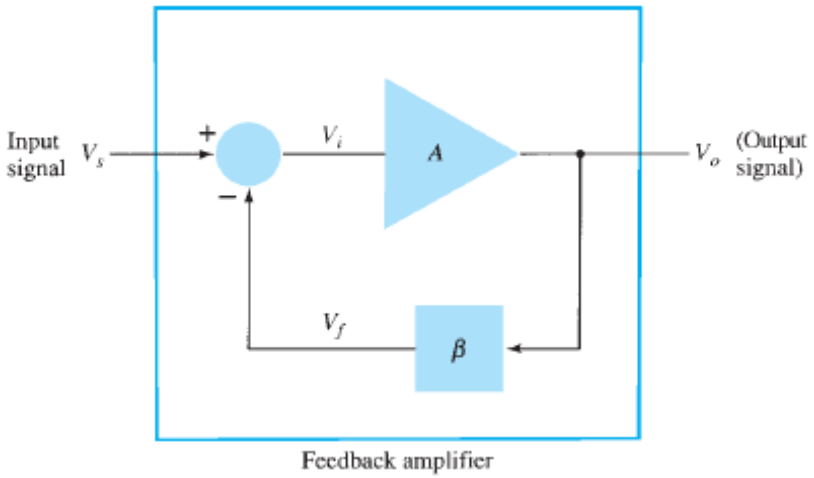
# MODULE – 5

## Feedback Amplifiers:

**Basic Feedback concept with simplified block diagram:**

Depending on the relative polarity of the signal being fed back into a circuit, one may have negative or positive feedback. Negative feedback results in decreased voltage gain, for which a number of circuit features are improved. Positive feedback drives a circuit into oscillation as in various types of oscillator circuits.

A typical feedback connection is shown below. The input signal $V_s$ is applied to a mixer network, where it is combined with a feedback signal $V_f$ . The difference of these signals $V_i$ is then the input voltage to the amplifier. A portion of the amplifier output $V_o$ is connected to the feedback network (β), which provides a reduced portion of the output as feedback signal to the input mixer network.




*Simple block diagram of feedback amplifier.*

If the feedback signal is of opposite polarity to the input signal, as shown in above Fig, results in negative feedback.

**Advantages of Negative feedback:**

- Higher input impedance.
- Better stabilized voltage gain.
- Improved frequency response.
- Lower output impedance.
- Reduced noise.
- More linear operation.

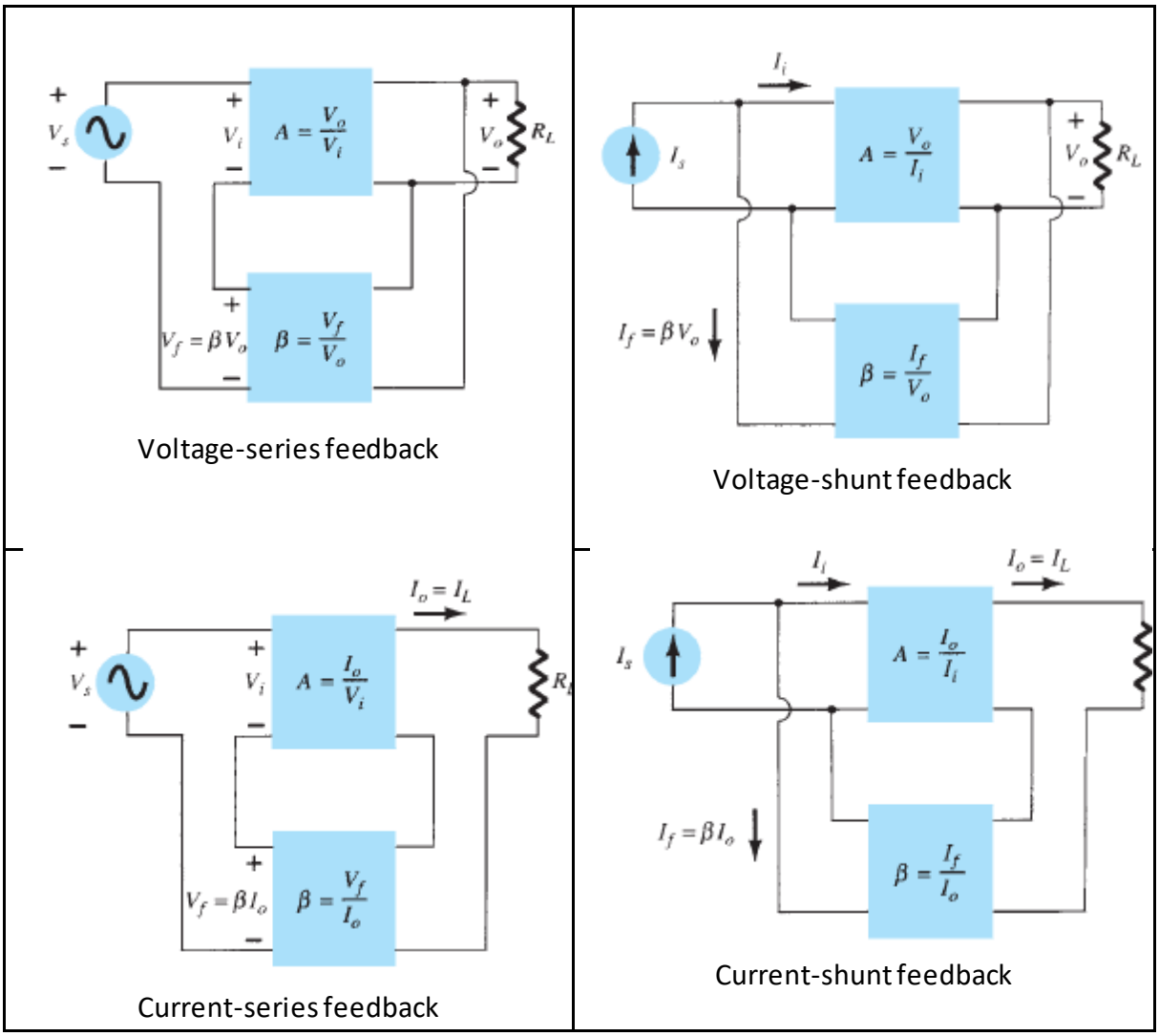
## FEEDBACK CONNECTION TYPES:

There are four basic ways of connecting the feedback signal. Both voltage and current can be fed back to the input either in series or parallel. Specifically, there can be:

1. Voltage-series feedback
2. Voltage-shunt feedback
3. Current-series feedback
4. Current-shunt feedback

In the list above, voltage refers to connecting the output voltage as input to the feedback network; current refers to tapping off some output current through the feedback network. Series refers to connecting the feedback signal in series with the input signal voltage; shunt refers to connecting the feedback signal in shunt (parallel) with an input current source.

**Feedback Topology:**




Series feedback connections tend to increase the input resistance, whereas shunt feedback connections tend to decrease the input resistance. Voltage feedback tends to

decrease the output impedance, whereas current feedback tends to increase the output impedance. Typically, higher input and lower output impedances are desired for most cascade amplifiers. Both of these are provided using the voltage-series feedback connection. We shall therefore concentrate first on this amplifier connection.

**Gain with Feedback**

The gain without feedback, A, is that of the amplifier stage. With feedback β, the overall gain of the circuit is reduced by a factor (1+Aβ), as detailed below. A summary of the gain, feedback factor, and gain with feedback of above feedback circuits are shown below.

| | | Voltage-Series | Voltage-Shunt | Current-Series | Current-Shunt |
|---|---|---|---|---|---|
| Gain without feedback | $A$ | $\frac{V_o}{V_i}$ | $\frac{V_o}{I_i}$ | $\frac{I_o}{V_i}$ | $\frac{I_o}{I_i}$ |
| Feedback | $\beta$ | $\frac{V_f}{V_o}$ | $\frac{I_f}{V_o}$ | $\frac{V_f}{I_o}$ | $\frac{I_f}{I_o}$ |
| Gain with feedback | $A_f$ | $\frac{V_o}{V_s}$ | $\frac{V_o}{I_s}$ | $\frac{I_o}{V_s}$ | $\frac{I_o}{I_s}$ |

*Summary of Gain, Feedback, and Gain with Feedback*

## Voltage-Series Feedback:

In the voltage-series feedback connection with a part of the output voltage fed back in series with the input signal, resulting in an overall gain reduction. If there is no feedback ($V_f = 0$), the voltage gain of the amplifier stage is

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i}$$

If a feedback signal $V_f$ is connected in series with the input, then

$$V_i = V_s - V_f$$

Since $$V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$$

then $$(1 + \beta A)V_o = AV_s$$

so that the overall voltage gain *with* feedback is

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}}$$

**Voltage-Shunt Feedback:**

The gain with feedback for the Voltage-Shunt Feedback network is

$$A_f = \frac{V_o}{I_s} = \frac{A\,I_i}{I_i + I_f} = \frac{A\,I_i}{I_i + \beta V_o} = \frac{A\,I_i}{I_i + \beta A\,I_i}$$

$$\boxed{A_f = \frac{A}{1 + \beta A}}$$

**Current-Series Feedback:**

The gain with feedback for the Current-Series Feedback network is

$$I_o = A \cdot V_i = A(V_S - V_f)$$
$$V_f = \beta \cdot I_o$$
$$A(V_S - \beta I_o) = I_o$$
$$A V_S = (1 + \beta A) I_o$$
$$A_f = \frac{I_o}{V_S} = \left(\frac{A}{1 + \beta A}\right)$$

**Current-Shunt Feedback:**

The gain with feedback for the Current-Shunt Feedback network is

$$A_f = \frac{I_o}{I_S} = \left(\frac{A}{1 + \beta A}\right)$$

**Note:** A summary of the effect of feedback on input and output impedance is provided in table shown below.

| Voltage-Series | Current-Series | Voltage-Shunt | Current-Shunt |
|---|---|---|---|
| $Z_{if}$ $Z_i(1 + \beta A)$ (increased) | $Z_i(1 + \beta A)$ (increased) | $\frac{Z_i}{1 + \beta A}$ (decreased) | $\frac{Z_i}{1 + \beta A}$ (decreased) |
| $Z_{of}$ $\frac{Z_o}{1 + \beta A}$ (decreased) | $Z_o(1 + \beta A)$ (increased) | $\frac{Z_o}{1 + \beta A}$ (decreased) | $Z_o(1 + \beta A)$ (increased) |

## Reduction in Noise and Nonlinear Distortion

Signal feedback tends to hold down the amount of noise signal (such as power-supply) and nonlinear distortion. The factor (1+ Aβ) reduces both input noise and resulting nonlinear distortion for considerable improvement. However, there is a reduction in overall gain (the price required for the improvement in circuit performance). If additional stages are used to bring the overall gain up to the level without feedback, the extra stage(s) might introduce as much noise back into the system as that reduced by the feedback amplifier. This problem can be somewhat alleviated by readjusting the gain of the feedback amplifier circuit to obtain higher gain while also providing reduced noise signal.

**Gain Stability with Feedback**

In addition to the b factor setting a precise gain value, we are also interested in how stable the feedback amplifier is compared to an amplifier without feedback.

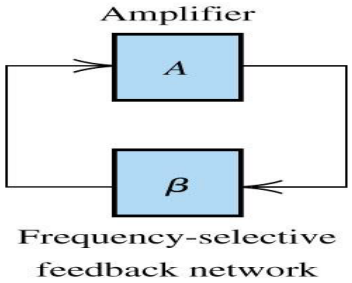
$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1 + \beta A|}\left|\frac{dA}{A}\right|$$

$$\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \qquad \text{for } \beta A \gg 1$$

This shows that magnitude of the relative change in gain $\left|\frac{dA_f}{A_f}\right|$ is reduced by the factor $|\beta A|$ compared to that without feedback $\left(\left|\frac{dA}{A}\right|\right)$.

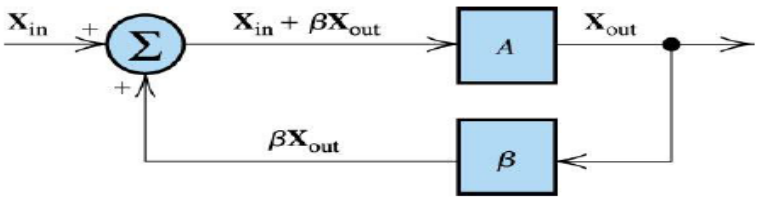
## Oscillator principle:

- Oscillators are circuits that generate periodic signals.
- An oscillator converts DC power from power supply to AC signals power spontaneously – without the need for an AC input source (Note: Amplifiers convert DC power into AC output power only if an external AC input signal is present.)
- There are several approaches to design of oscillator circuits. The approach to be discussed is related to the feedback using amplifiers. A frequency-selective feedback path around an amplifier is placed to return part of the output signal to the amplifier input, which results in a circuit called a linear oscillator that produces an approximately sinusoidal output.
- Under proper conditions, the signal returned by the feedback network has exactly the correct amplitude and phase needed to sustain the output signal.




**The Barkhausen Criterion:**

Typically, the feedback network is composed of passive lumped components that determine the frequency of oscillation. So, the feedback is complex transfer function, hence denoted as β(f). We can derive the requirements for oscillation as follows: initially, assume a sinusoidal driving source with phasor Xin is present. But we are interested in derive the conditions for which the output phasor Xout can be non-zero even the input Xin is zero.



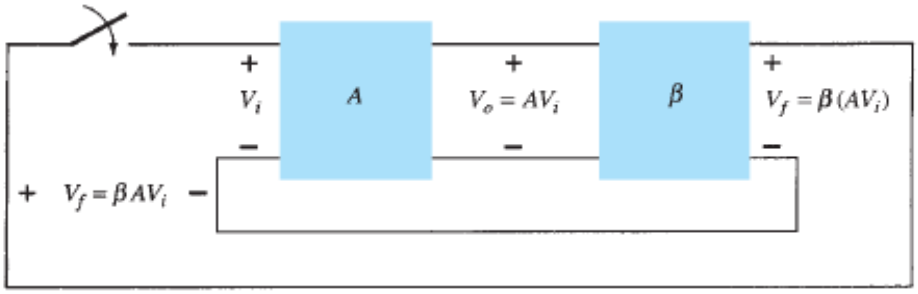

The output of the amplifier block can be wrtten as $X_{out} = A(f)[X_{in} + \beta(f)X_{out}]$

solve for $X_{out,}$ we obtain $X_{out} = \dfrac{A(f)}{1 - A(f)\beta(f)} X_{in}$

If $X_{in}$ is zero, the only way the the output can be nonzero is to have $A(f)\beta(f) = 1$

The above condition is know as Barkhausen Criterion.

**Basic Feedback circuit used as an oscillator:**

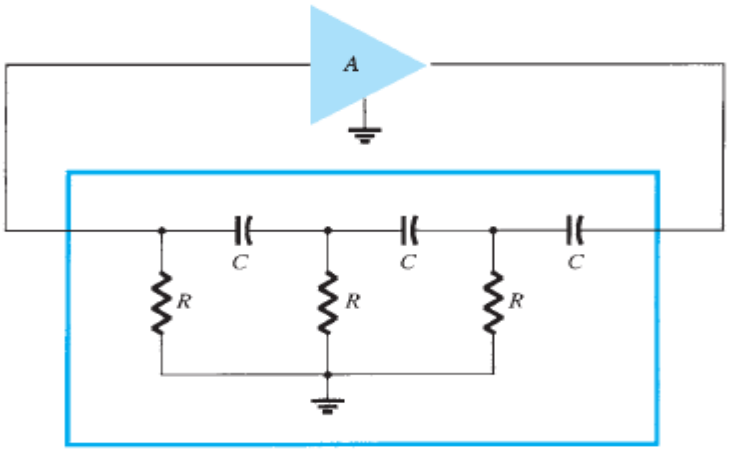



(*Feedback circuit used as an oscillator)*

## RC - PHASE-SHIFT OSCILLATOR:

An example of an oscillator circuit that follows the basic development of a feedback circuit is the RC- *phase-shift oscillator.* An idealized version of this circuit is shown in Fig. below. Recall that the requirements for oscillation are that the loop gain *Aβ* is greater than unity *and* that the phase shift around the feedback network is 180° (providing positive feedback). In the present idealization, we are considering the feedback network to be driven by a perfect source (zero source impedance) and the output of the feedback network to be connected into a perfect load (infinite load impedance). The idealized case will allow development of the theory behind the operation of the RC-phase-shift oscillator.

**Basic Block Diagram of RC-Phase shift Oscillator:**




(Idealized RC- phase-shift oscillator)

Concentrating our attention on the phase-shift network, we are interested in the attenuation of the network at the frequency at which the phase shift is exactly 180°. Using classical network analysis, we find that

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$\beta = \frac{1}{29}$$

and the phase shift is 180°.

When considering the operation of the feedback network, one might select the values of R and C to provide (at a specific frequency) $60^0$phase shift per section for three sections, resulting in a 180° phase shift, as desired. This, however, is not the case, since each section of the RC in the feedback network loads down the previous one. The net result that the total phase shift be 180° is all that is important. The frequency given is that at which the total phase shift is 360°.

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