Basic Electronics :- (BE)

Amulya Ku. Roul.

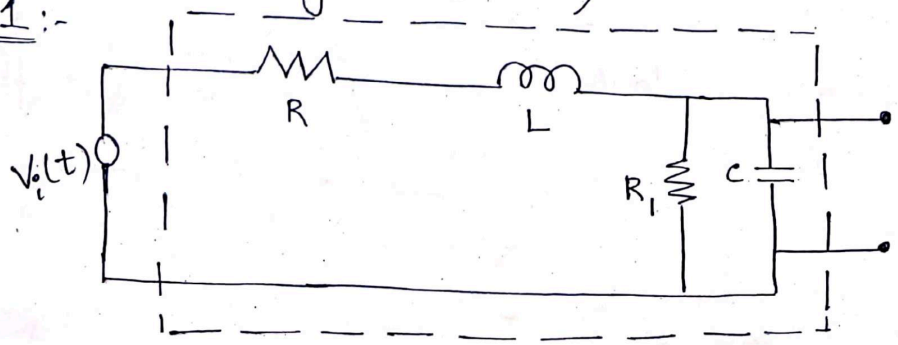
Electrical	Electronics
→ Electrical device is made up of the material like conductors.	→ Electronics devices are made up of materialise semi-conductor. (ex- Si, Ge...)
→ The power level or voltage level in electrical is very large. (220 v peak voltage).	→ The power level or voltage level in electronics is very small (in mili volt range mV)
→ The frequency of operation of electrical circuit is very small. (50 Hz or 60 Hz)	→ The frequency of operation of electronics circuit is very large. (MHz, GHz, THz :) $\downarrow 10^6$ $\downarrow 10^9$ $\downarrow 10^{12}$
→ The size of electrical devices is very large.	→ The size of the electronics devices is very small.

Signal :-

→ Signal is a physical quantity, which is function of one or more than one independent variable like 't' or special variable. (x, y, z, ...).

Example:- voltage, current, power, temperature, distribution, speech signal, image signal, video signal. (Audio)

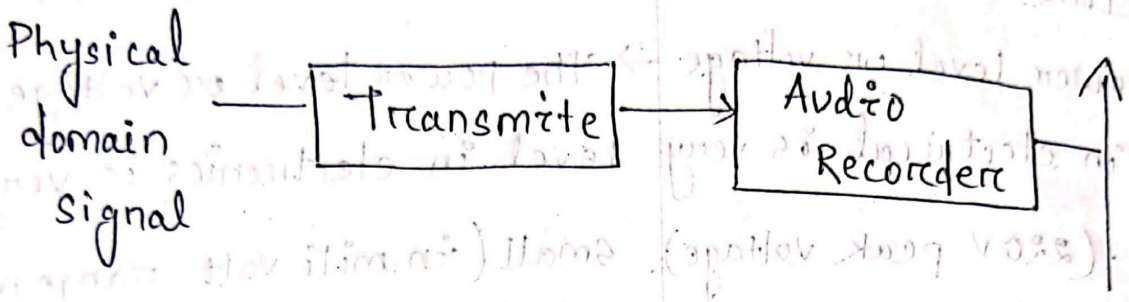
Ex-1 :-



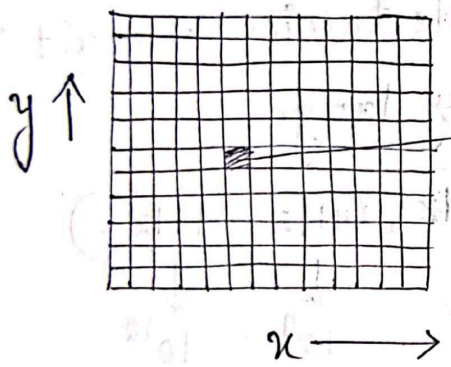
The output of electrical circuit consisting of a passive element like resistance, conductor and inductor may be sinousuidal signal.

$$V_o(t) = V_m \sin \omega_o t$$

Ex: 2 :-



Ex: 3 :-



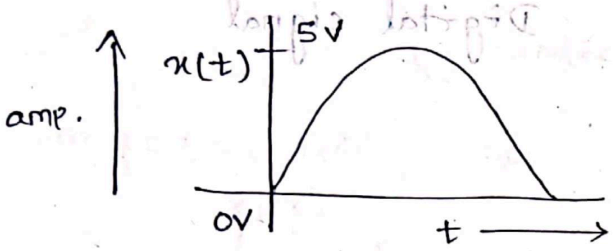
Text Book :-

1. Electronics Device & Circuit by Boyelstats. (EDC)
2. Micro-electronics by sedra & Smith.
3. Electronics device & circuit by Milliman and Haiknis.

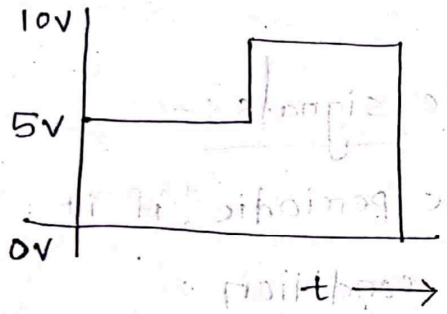
Analog signal & digital signal :-

14/08/2019

→ A signal is said to be analog signal, if the signal having an infinite no. of amplitude levels or amplitude states.

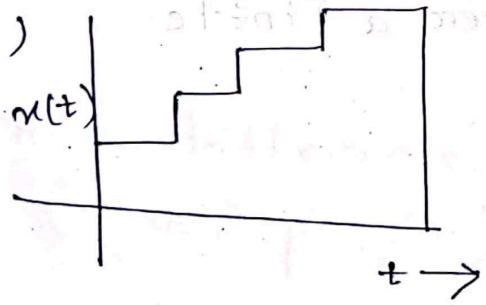


→ A signal is said to be a digital signal, if the signal is having a finite no. of amplitude levels or amplitude states.



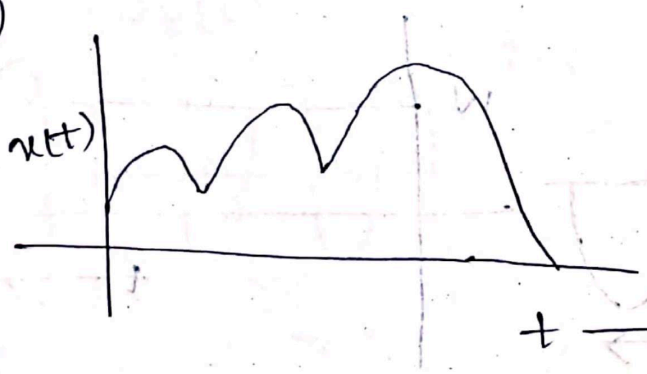
Q:- classify the following signal as analog and digital signal.

(i)



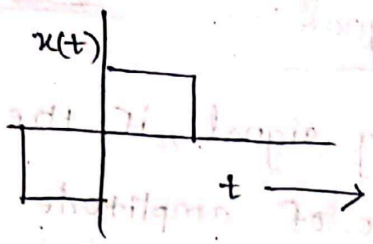
Digital signal

(ii)



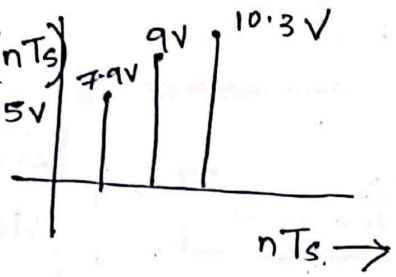
Analog signal.

(iii)



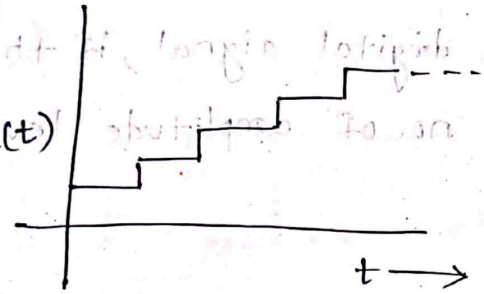
Digital signal

(iv)



Digital signal

(v)



Analog signal.

Periodic and non-periodic signals :-

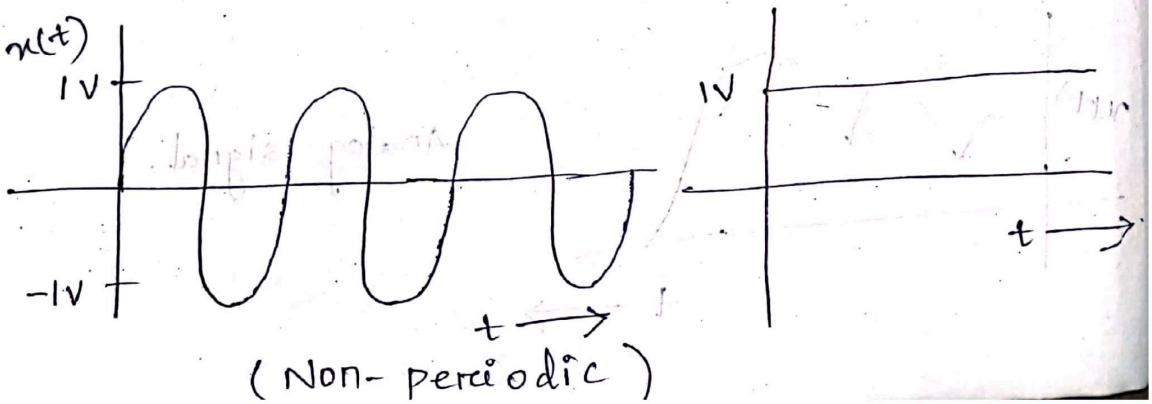
→ A signal is a said to be periodic, if it satisfies the following condition :-

① Signal must be everclasting. (i.e; it must exists from $-\infty$ to $+\infty$.)

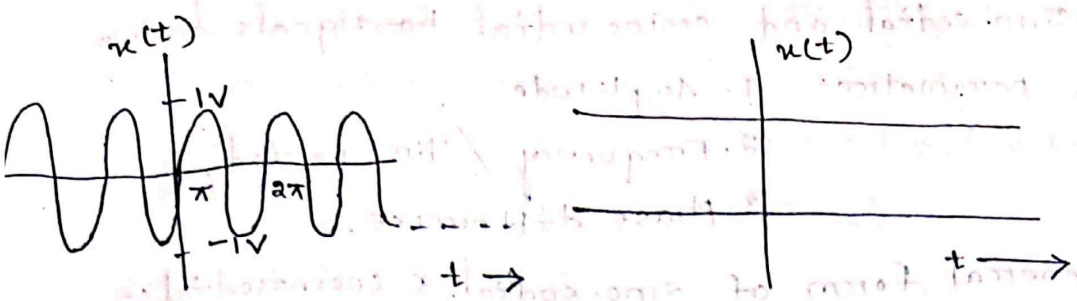
② It should be repeated over a finite interval of time.

Otherwise, non-periodic.

Ex:-

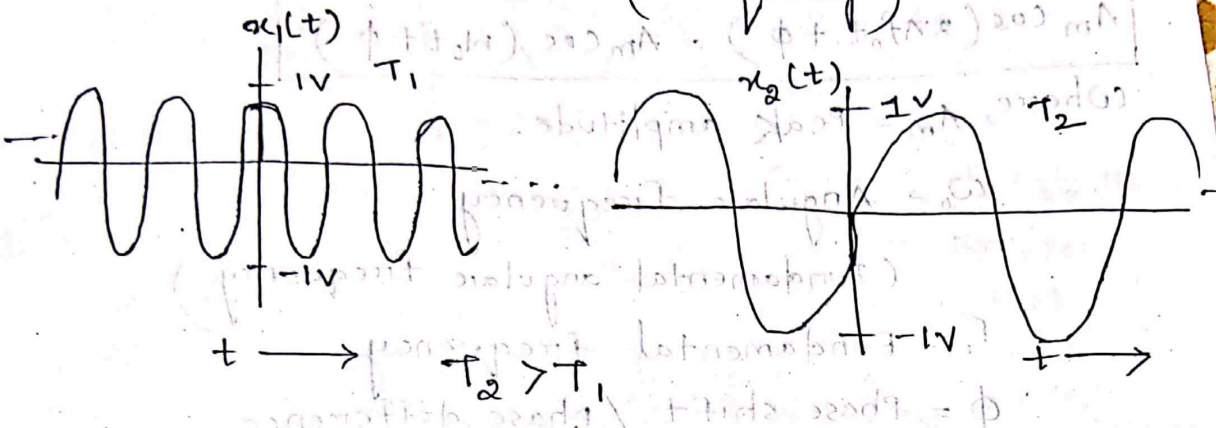


(Non-periodic)



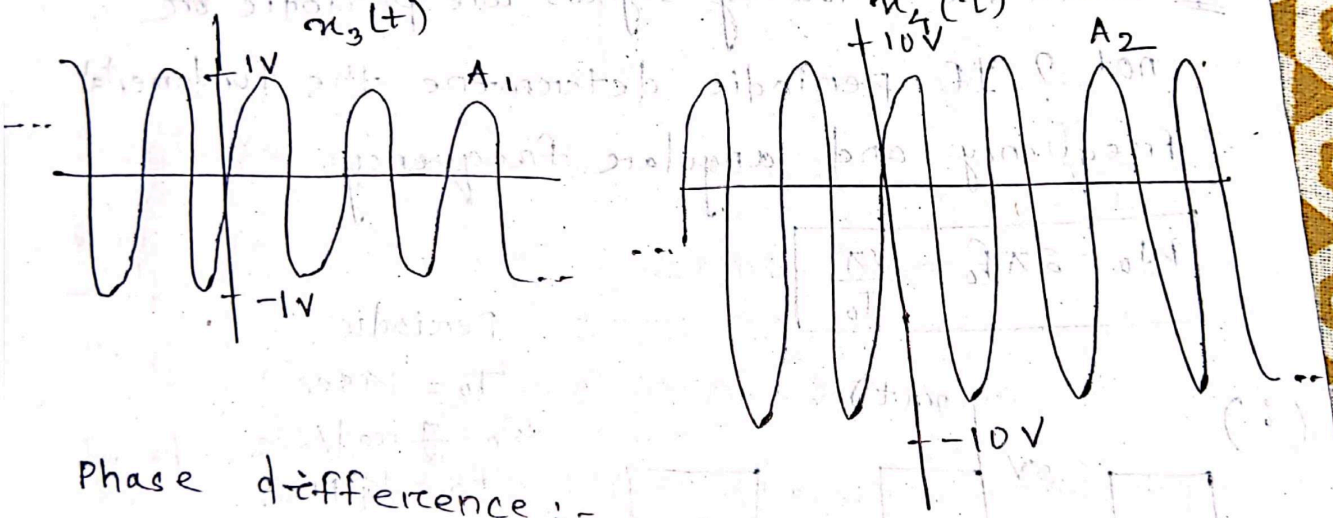
(Periodic)

Time period difference :- (Frequency)

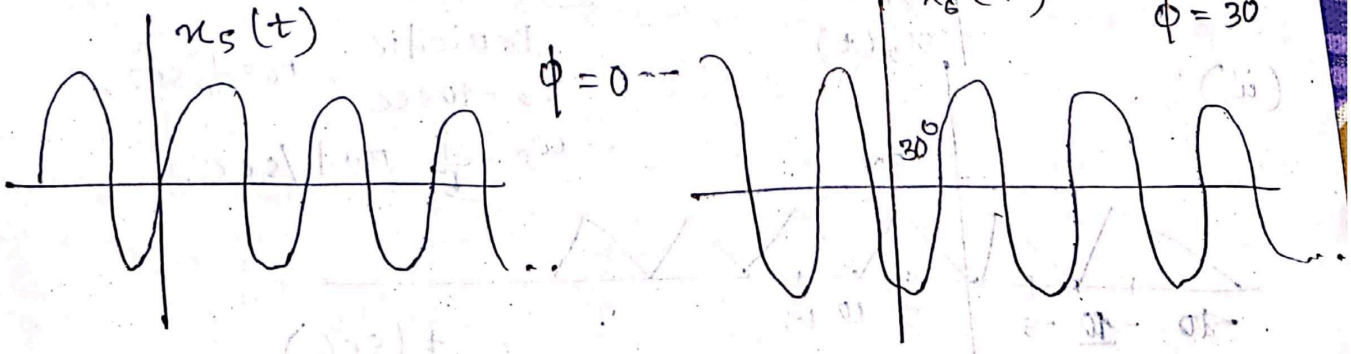


$T_2 > T_1$

Amplitude difference :-



Phase difference :-
(starting point)



(*) Sino-sodial and cosinosodial ~~so~~ signals having 3 parametres. 1. Amplitude
2. Frequency / Time period.
3. phase difference..

General form of sino-sodial & cosinosodial :-

~~$A_m \sin(2\pi f_0 t)$~~

$$A_m \sin(2\pi f_0 t + \phi) = A_m \sin(\omega_0 t + \phi)$$
$$A_m \cos(2\pi f_0 t + \phi) = A_m \cos(\omega_0 t + \phi)$$

where, A_m = Peak amplitude.

ω_0 = Angulare frequency
(Fundamental angulare frequency)

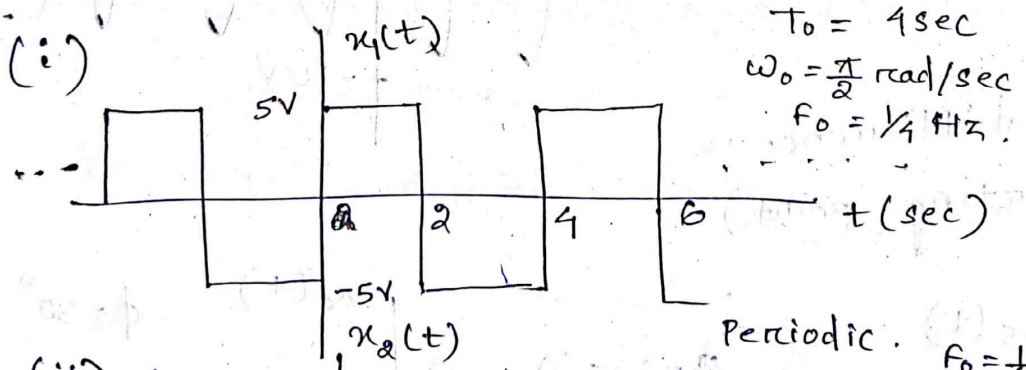
F_0 = Fundamental frequency

ϕ = Phase shift / phase difference

Q:- check the following signals are periodic or not ? If periodic determine the fundamental frequency and angulare frequency.

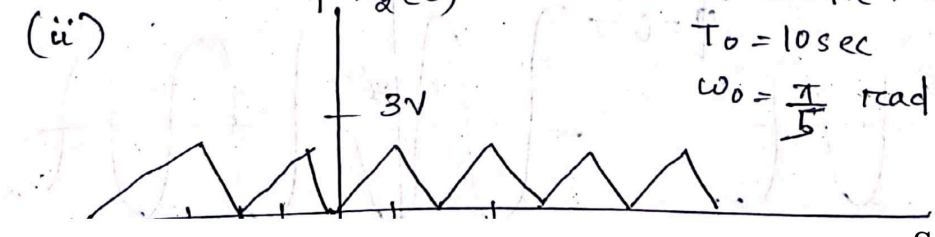
$$\omega_0 = 2\pi f_0 = \frac{2\pi}{T_0}$$

(i)

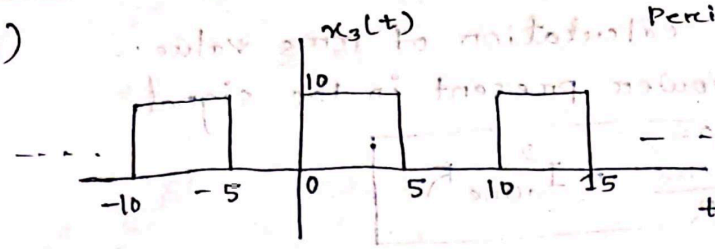


Periodic.
$T_0 = 4$ sec
$\omega_0 = \frac{\pi}{2}$ rad/sec
$f_0 = 1/4$ Hz.

(ii)



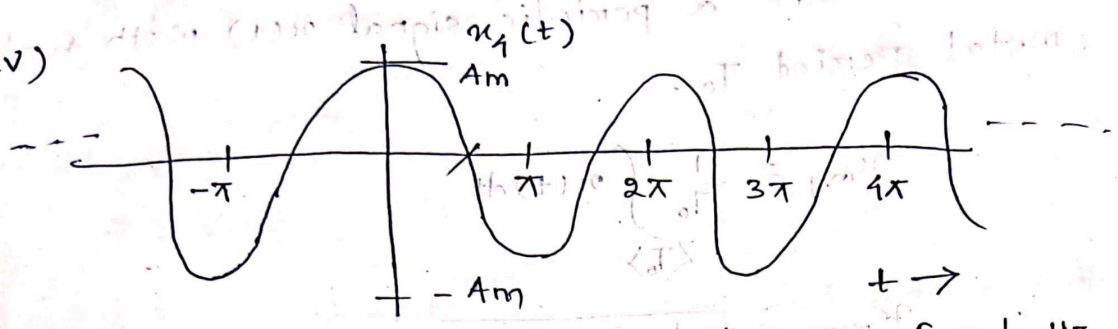
Periodic.
$T_0 = 10$ sec
$\omega_0 = \frac{\pi}{5}$ rad/sec.
$f_0 = \frac{1}{10}$ sec.

(iii) 

Periodic $T_0 = 10$ sec

$f_0 = \frac{1}{10}$ sec.

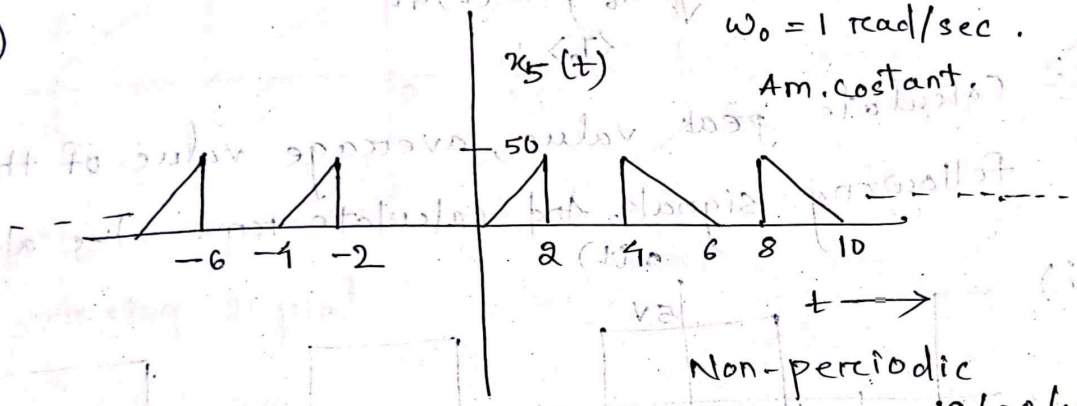
$\omega_0 = \frac{\pi}{5}$ rad/sec

(iv) 

$T_0 = 2\pi$, $f_0 = \frac{1}{2\pi}$ Hz

$\omega_0 = 1$ rad/sec.

Am. costant.

(iv) 

Non-periodic

19/08/19

Calculation of peak value, average value and R.M.S value of any periodic signal :-

Significance of calculation of peak value :-

→ It gives maximum power present in the signal.

Significance of calculation of avg. value :-

→ It gives the total dc power present in the signal.

$$P_{dc} = \frac{V_{avg}^2}{R} = I_{Avg}^2 R$$

Similarly,

$$P_{peak} = \frac{V_p^2}{R} = I_p^2 R$$

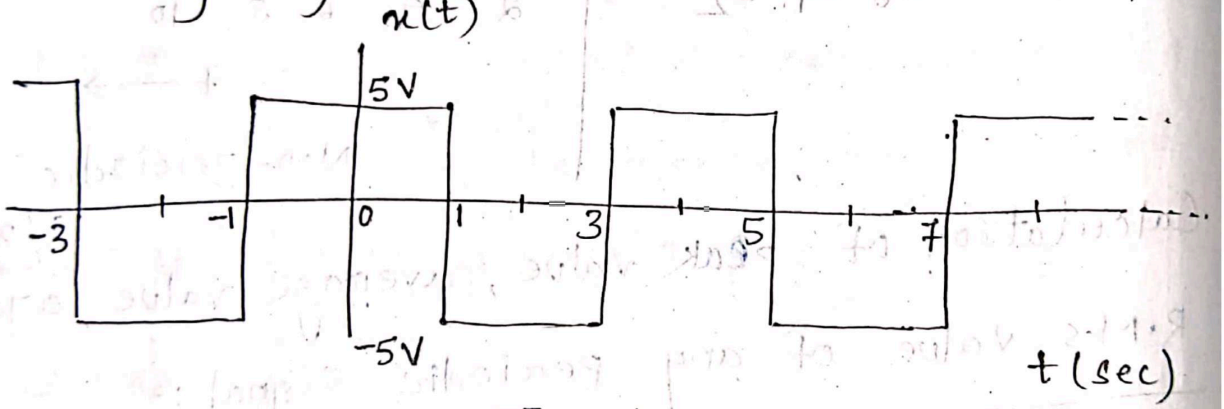
Let's consider a periodic signal $x(t)$ with fund-metal period T_0.

$$x_{avg} = \frac{1}{T_0}\int_{\langle T_0 \rangle} x(t)\,dt$$

$$x_{rms} = \sqrt{\frac{1}{T_0}\int_{\langle T_0 \rangle} x^2(t)\,dt}$$

Q:- Calculate peak value, average value of the following signals. And calculate rms value also.

(i)



$T_0 = 4$ sec.

$x_{peak} = 5V$ (Periodic signal) - digital signal

$$x_{avg} = \frac{1}{T_0}\int_0^4 x(t)\,dt$$

$$= \frac{1}{4}\int_0^4 x(t)\,dt$$

$$= \frac{1}{4}\left[\int_0^1 5t\,dt + \int_1^3 (-5)t\,dt + \int_3^4 5t\,dt\right]$$

$$= \frac{1}{4}\left[5 + (-10) + 5\right] = \frac{1}{4} \times 0 = 0\,V$$

$$x_{rms} = \sqrt{\frac{1}{4}\int_0^4 x^2(t)\,dt}$$

$$= \sqrt{\frac{1}{4}\left(\int_0^1 25\,dt + \int_1^3 25\,dt + \int_3^4 25\,dt\right)}$$

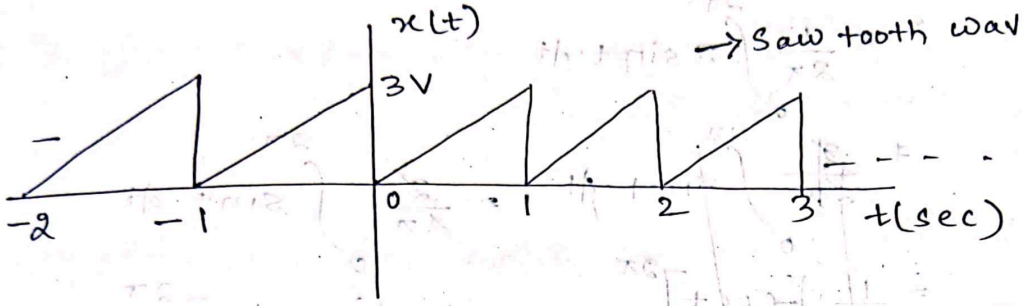
$$= \sqrt{\frac{1}{4}\left(25 + 50 + 25\right)}$$

$$= \sqrt{\frac{1}{4} \times 100}$$

$$= \sqrt{25}$$

$= 5\ V$.

(ii)



→ Saw tooth wave.

$T_0 = 1\ sec$

Analog signal.

Here, $y = mx + c$ (c = 0)

$\therefore x(t) =$

$x_{peak} = 3\ V$

$$x_{avg} = \frac{1}{1}\int_0^1 x(t)\,dt$$

$$= \int_0^1 3t \cdot dt$$

$$= 3\,\frac{t^2}{2}\Big]_0^1$$

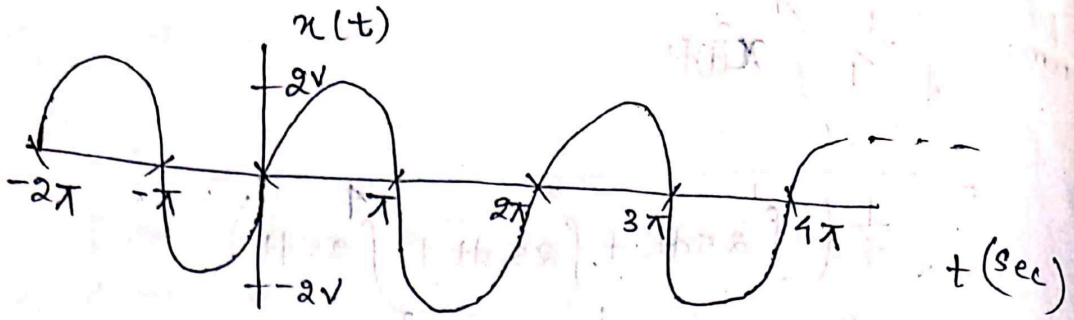
$$= \frac{3}{2}\ V.$$

$$x_{rms} = \sqrt{\frac{1}{T_0}\int_0^{T_0} x^2(t)\,dt} = \sqrt{\frac{1}{1}\int_0^1 (3t)^2\,dt}$$

$$= \sqrt{\int 9t^2\,dt\Big]_0^1} = \sqrt{3(1)^3}$$

$= \sqrt{3}\ V$ Ans

(iii)



$T_0 = 2\pi$ sec.

$x_{peak} = 2V$. $f_0 = \frac{1}{2\pi}$.

$A_m \sin \omega_0 t$
$2 \sin t$

$\therefore \omega_0 = 2\pi f_0$

$= 2\pi \times \frac{1}{2\pi} =$

$$x_{avg} = \frac{1}{2\pi} \int_0^{2\pi} x(t)\, dt$$

$$= \frac{1}{2\pi} \int_0^{2\pi} 2 \sin t \cdot dt$$

$$= \frac{2}{2\pi} \int_0^{2\pi} \sin t \cdot dt$$

$$= \frac{1}{\pi} \left[-\cos t\right]_0^{2\pi}$$

$$= \frac{1}{\pi} \left[-\cos t\right]_0^{2\pi}$$

$$= -\frac{1}{\pi} \cos(2\pi + 0) = -\frac{1}{\pi} \left[\cos 2\pi - \cos 0\right]$$

$$= -\frac{1}{\pi} \cos 2\pi = -\frac{1}{\pi} [1 - 1] = 0\,V$$

Ans

OR

$$= \frac{1}{2\pi} \left[\int_0^{\pi} 2 \sin t \cdot dt + \int_{\pi}^{2\pi} 2 \sin t \cdot dt \right]$$

$$= \frac{1}{2\pi} \left[2 \left[-\cos t\right]_0^{\pi} + 2 \left[-\cos t\right]_{\pi}^{2\pi} \right]$$

$$= \frac{1}{2\pi} \cdot 2 \left[-\{\cos \pi - \cos 0\} + \{\cos 2\pi - \cos \pi\} \right]$$

$$= \frac{1}{\pi} \left[-(-1+1) + (1-1) \right]$$

$$= \frac{1}{\pi} \times 0$$

$$= 0\,V$$

$$x_{rms} = \sqrt{\frac{1}{T_0}\int_{\langle T_0 \rangle} x^2(t)\,dt}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} 1\sin^2 t\,dt}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \frac{1-\cos 2t}{2}\,dt}$$

$$= \sqrt{\frac{1}{2\pi}\left(\int_0^{2\pi}\frac{1}{2}\,dt - \int_0^{2\pi}\frac{\cos 2t}{2}\,dt\right)}$$

$$= \sqrt{\frac{1}{2\pi}\left(\frac{1}{2}\times(2\pi-0) - \frac{1}{2}\,\frac{\sin 2t}{2}\right]_0^{2\pi}}$$

$$= \sqrt{2} \text{ Volt.}$$

Note-1

$A_m \sin 2\pi f_0 t$ or $A_m \sin \omega_0 t$

Peak value $= A_m$

$x_{avg} = 0$

$x_{rms} = \frac{A_m}{\sqrt{2}}$

Note-2

$A_m \cos 2\pi f_0 t$ or $A_m \cos \omega_0 t$

Peak value $= A_m$

$x_{avg} = 0$

$x_{rms} = \frac{A_m}{\sqrt{2}}$

$$\boxed{x_{avg} = \frac{1}{T_0}\int_0^{T_0} x(t)\,dt}$$

$$= \frac{\text{Area under } x(t)}{T_0}$$

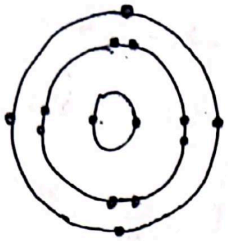
If area is 0, then $x_{avg} = 0$.

21/08/19

Semiconductor Material :-

→ Valency 4 elements like Si, Ge are used as semiconductor material.

$Si_{14} \rightarrow 1s^2, 2s^2\ 2p^6\ 3s^2\ 3p^6$ → Electronic configuration of Si atom.



(Atmoic str of Si atom)

→ Conduction is possible when the e^- is free from the nucleus i.e; free e^- can produce conduction.

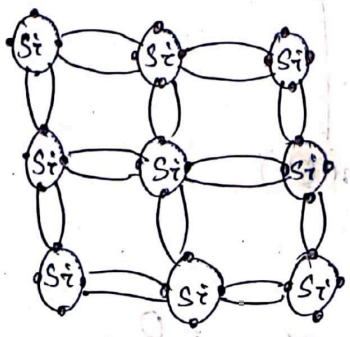
→ Outermost shell e^- can be free from nucleus. i.e; Outermost e^-, when they will free from the nucleus can provide conduction.

→ The inner shell e^-, never be free from the nucleus and this inner shell e^- always bound e^-, they never produce conduction.

$Ge_{32} \rightarrow 1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^{10}\ \boxed{4s^2\ 4p^2}$.

Covalent Bond :-

It is formed by sharing of e^- betn 2 atoms.



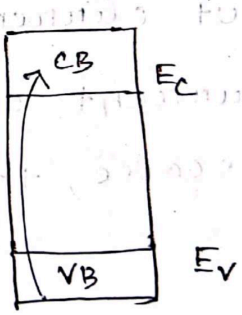
Silicon Crystal.

→ In si crystal only a large no. of si atoms are present, each atom tries to get stability, by sharing the e^- with the neighbouring atoms. such that each atoms will get 8 e^- in the outermost shell by sharing the e^-. As a result, formation of covalent bond.

→ The e^- which are present in the covalent bond aren't free e^- and they aren't produce the conduction, bcoz the conduction is bcoz of the free e^-.

→ To increase the conductivity of the si crystal we should increase the temperature. By increasing the sufficient temp. some of covalent bonds are break as a result, there will be generation of equal no. of free e^- and ~~volts.~~ holes.

→ When the covalent bond will break, e^- will move from valency band to conduction band & the e^- becomes free.



Concept of hole:-

→ The absence of e^- in covalent bond, is known as hole.

→ Hole is +ve ~~as~~ and charge of it 1.6×10^{19} C.

Note:-

→ The si crystal consists ~~upon~~ of only the si atoms. So, it is known as pure semi-conductor or intrinsic semiconduct.

→ In it, No. of hole = No. of free e^- i.e in

pure semiconductor, $\boxed{n = p}$

electron conc. = hole conc.

Here, $\sigma_n = nq\mu_n$, $\sigma_p = nq\mu_p$

Conductivity due to e^- is defined as $nq\mu_n$ and conductivity due to hole is known as $nq\mu_p$.

p = Conc. of hole, μ_n = Mobility of e^-

n = Conc. of e^-, μ_p = Mobility of hole.

Always $\boxed{\mu_n > \mu_p}$

Note -:

In intrinsic semiconductor,

$\sigma_n > \sigma_p$ $(\because \mu_n > \mu_p)$

so, $I_n > I_p$

22/08/19

→ In intrinsic semiconductor,

electron conc. = hole conc.

But current due to free e^- is greater than current due to hole.

Because, the mobility of free e^- > mobility of hole.

$J = \sigma E$

$J_n = \sigma_n E$

$\frac{I_n}{A} = nq\mu_n E$

$\Rightarrow \boxed{I_n = nq\mu_n EA}$

∴ Here Total current(I)

$\boxed{I = I_n + I_p}$

Again, $J_p = \sigma_p E = nq\mu_p E$

$\Rightarrow \boxed{I_p = nq\mu_p EA}$

In intrinsic S.C, $n = p$, $\mu_n > \mu_p$ and $I_n > I_p$.

→ To increase the conductivity, by increasing the temp. of intrinsic semiconductor isn't a good soln. So, increase the conductivity we should go for dopping concept.

→ Dopping means addition of impurities to pure/intrisic semiconductor.

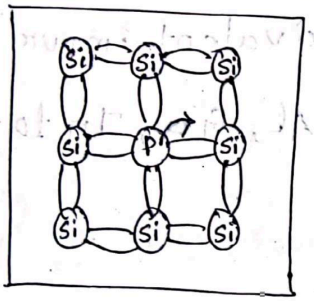
⇒ By addition of impurities to pure/intrisic s.c becomes extrinsic s.c.

Extrinsic semi-conductor:-

1 : 10^8

- n-type s.c [P, A, A, B]
- P-type s.c [B, A, G, I]

(i) n-type semi-conductor:-



→ It is form by addition of pentavalent impurities (donor impurities) like P, As, ~~Ab~~ Sb, Bi.

→ By Addition of pentavalent impurities into pure s.c, the pentavalent impurity become octate by sharing $4e^-$ of neighbouring Si atom. As a result one free e^- will be left out from the pentavalent impurities outermost shell. This e^- will be filled which will take part in conduction.

→ Total conductivity in n-type s.c is because of conductivity due to free e^- & the holes.

so, $\boxed{I = I_n + I_p}$

$J_n = \sigma_n E$ $\quad J_p = \sigma_p E$

$I_n = \sigma_n E A$ $\quad I_p = \sigma_p E A$

$= n q \mu_n E A$ $\quad = n q \mu_p E A$

$\therefore I_n >> I_p$.

Note :-

→ In n-type s.c, the majority carriers is e^- & minority carriers is hole.

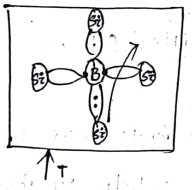
→ In n-type s.c, the majority current is e^- current (I_n) and minority current is hole current (I_p)

$\boxed{I_n >> I_p}$.

(ii) P-type semi-conductor :-

→ It is form by addition of trivalent impurities (acceptors impurities) like B, Al, Ga, In to the intrinsic s.c / pure s.c.

→



$\boxed{P_p >> n_p}$

$I = I_p + I_n$

$= J_p A + J_n A$

$= \sigma_p E A + \sigma_n E A$

$= \uparrow P_p q \mu_p \uparrow E A + \downarrow n_p q \mu_n \uparrow E A$

↑gain ; $\delta_p > \delta_n$

$\Rightarrow J_p > J_n$

$\Rightarrow I_p > I_n$

Note :-

→ Hole is majority carriers and e^- is minority carriers.

→ Hole current is majority and e^- current is

minority. Hence $\boxed{I = I_p + I_n}$

Here doping effect is more than mobility effect.

26/08/2019

Pauli's exclusion principle:-

→ Each e^- should have unique energy level. (No two e^- will have same energy level).

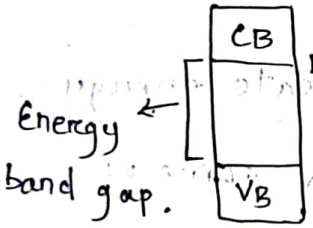
Energy Band:-

→ It is the collection of closely spaced energy level.

Energy Band

Classification of materials based on energy band:-

① Insulator ② Conductor ③ Semi-conductor.



$E_g = E_c - E_v$

E_c = Lowest energy level in conduction band.

E_v = Highest energy level in valency band.

$E_c - E_v$ = Energy band gap. (E_g).

Insulator:-

→ In case of insulator, the energy band gap is very large, so by thermal excitation, so no e^- will move from valency band to conduction band. Hence there is no free e^- available in conduction band. So, there will be no conduction in case of insulator.

Conductivity (σ) = 0

$\Rightarrow \sigma = 0$

$\Rightarrow \rho = \frac{1}{\sigma} = \infty$ (Resistivity)

$\boxed{I = 0}$

Conductor:-

→ In case of conductor, valency band & conduction band overlap each other. So, a large no. of free e^- available in CB. Hence conductivity

$n \neq 0$

$\Rightarrow \sigma \neq 0$ (large)

$\Rightarrow \rho = \frac{1}{\sigma} \neq \frac{1}{0}$ (small)

$\boxed{I \neq 0}$

Semi-conductor:-

→ In case of this, there is moderate energy gap. So, by thermal excitation some of covalent bond will break & some e^- will move from VB to CB. As a result a moderate no. of free e^-s and holes will be available.

Here $\sigma \neq 0$ (moderate)

$\Rightarrow \rho \neq \frac{1}{\sigma} \Rightarrow \rho \neq \frac{1}{0}$ (moderate)

$\Rightarrow \boxed{I \neq 0}$

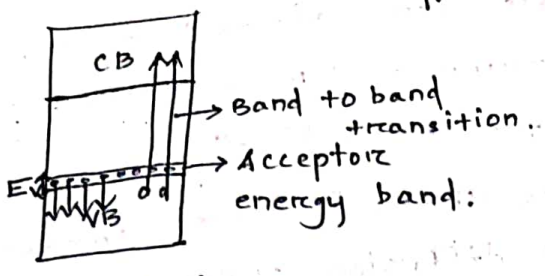
$\boxed{I = I_n + I_p}$

Note:-

→ All intrinsic or extrinsic SC at 0°K are behaved like insulator.

P-type SC

1.



(at 0° K)

$P=0$, $\sigma=0$

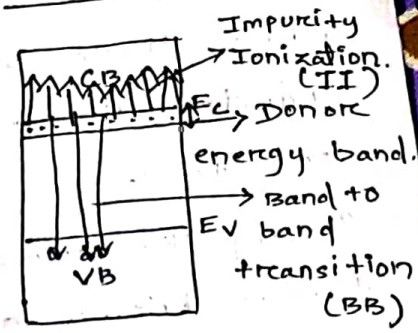
$\rho=\infty$, $I=0$

(at 50K)

(at 300K)

N-type S.C

1.



(at 0° K)

$n \neq 0$, $\sigma \neq 0$

$\rho \neq \infty$, $I \neq 0$

(at 50K)

(at 330K)

Hence; $\boxed{I = I_{BB} + I_{II}}$

$\Rightarrow I = I_{p(BB)} + I_{n(BB)} + I_{II(n)}$

$= I_p + I_n$ (In N-type sc)

But; $\boxed{I = I_{BB} + I_{II}}$

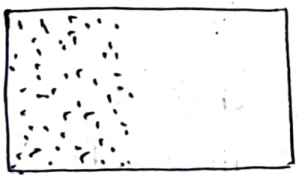
$= I_{n(BB)} + I_{p(BB)} + I_{p(II)}$

$= I_n + I_p$. (In P-type sc)

28/08/19

Diffusion and Drift phenomenon :-

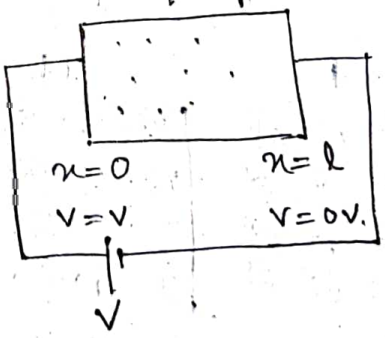
N-type S.C



$x=0$ $\quad$ $x=l$

$n=n_1$ $\quad$ $n=n_2$

P type S.C



$n_1 > n_2$

$\frac{dn}{dx} \neq 0$, $\frac{dn}{dx} = \frac{n_2 - n_1}{l - 0}$

→ Diffusion is a natural occuring phenomena, when there exists conc. gradient in semi-conductor, the carriers will move from higher conc to lower conc. autometically.

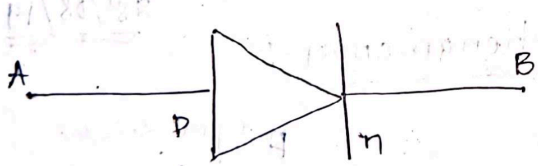
→ During this process, there is some current, this is known as diffusion current.

→ When there exist potential gradient in semi-conductor carriers will move inside the semi-conductor, this process is known as drift process.

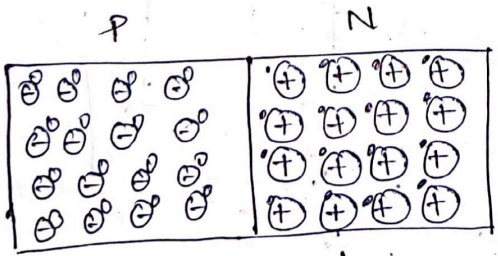
→ When there exist potential gradient, carriers will move inside the s.c: Bcoz of the movement of carriers inside the s.c, there are be some current inside the s.c is called drift current.

P-n junction diode :-

Eg: Schematic diagram :-



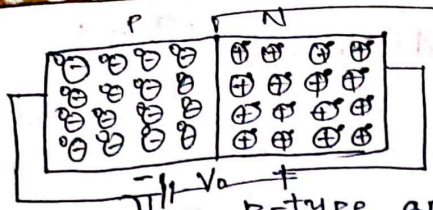
(diode)



(It acts like a capacitance effect)

— V_0 +

↳ Barrier potential / Contact ~~pot~~ point.



→ When p-type and n-type s.c bcoz of diffusion process e^- will move from n-type s.c and hole will move from p-type to n-type s.c.

→ As a result hole ~~with~~ e^- pair will disapear at the junction. After some time, diffusion will stop. Cox generated -ve plate in p-type s.c will repel the e^- will n-type s.c and generated +ve plate in n-type s.c will repel the e^- will p-type s.c.

Note:

① Junction allows the flow of minority character, but it opposes flow of majority character.

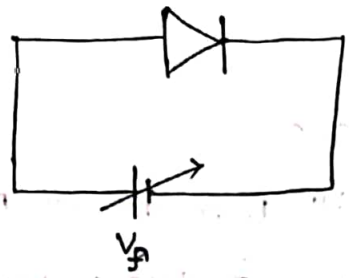
② Inside the p-n junction, a -ve plate is generated in p-side & +ve plate is in n-side.

④ At +ve plate there are some +ve potential. and -ve " " " " +ve potential. Inside the junction there will be some potential diff. betⁿ p type s.c & n-type s.c. This is called contact potential or Barrier potential.

$V_0 = 0.7V$ (Si)

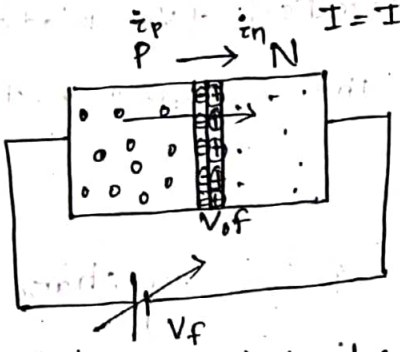
$V_0 = 0.3V$ (Ge)

Forward Bias of PN Junction diode:-



→ When PN Junction diode is connected to an external DC voltage, such a manner that, P side of the diode is connected to +ve plate of the supply and N side of diode is connected to -ve plate of the supply.

→ The diode is said to be forward biased.



→ When $V_f < 0.7V$, less amount of current will flow, because of ~~minority~~ ~~character~~, minority carrier.

→ When $V_f > 0.7V$, for si, majority carrier will diffuse across the junction.

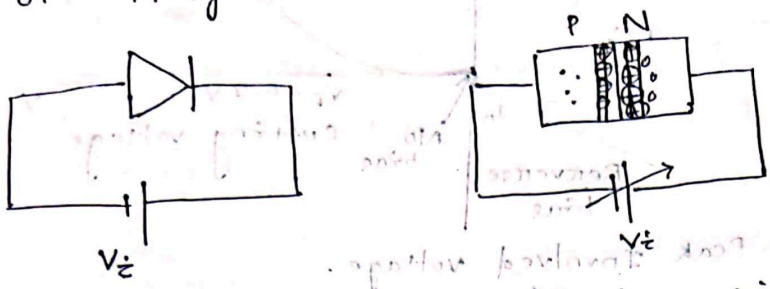
As a result, a diffusion part will flow from P side to N side.

→ But, increasing V_f beyond 0.7 V, diffusion current will decrease, because more no. of carrier diffuse across the junction.

→ the nature of the increasing current, by increasing V_f is exponential. (Experimentally proved.)

Reverse Bias of PN Junction diode :-

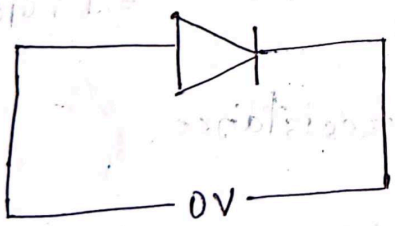
→ A PN Junction diode is said to be reverse bias, when P-side of diode is connected to -ve plate of supply & N-side is connected to +ve.



→ By increasing V_i, depletion region width will increase, there will be no flow of mejority carriers across the junction, only the minority carriers will drift across the junction.

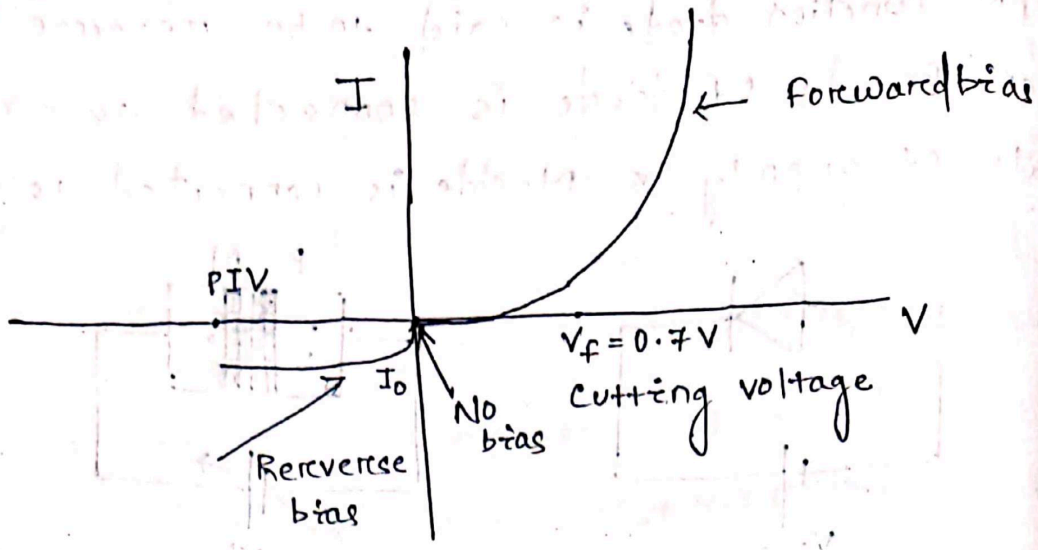
→ The net current across the junction is because of only the drifting of minority carriers which is flow from N side - P side.

→ The diode is said to be under no bias condition, when no external bias voltage is applied across the PN junction.



→ During no bias condition, there will be no flow of majority carriers across the junction.

→ There will be existance of deplition region across the junction.



PIV - Peak Involved voltage.

$I \rightarrow I_o \left(e^{V_D}\right)$

Diode current voltage :-

$$I = I_o \left(e^{V_D/nV_T} - 1 \right)$$

Where, V_D = voltage across the diode → +ve for FB
→ -ve for RB

I_o = Reverse saturation current

I = Current across diode.

V_T = temperature equivalent voltage = $\frac{T \text{ in } ^\circ K}{11600}$

At 300 °k, 27°C

$V_T = 25\,mV$ or $26\,mV$.

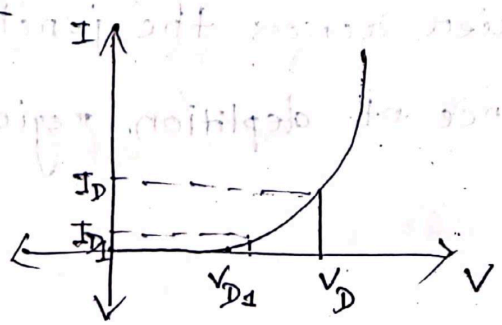
$\eta = 2$, Si
$= 1$, Ge
} constant

Diode resistance level :-

(a) DC resistance or static resistance.

(b) AC or dynamic resistance :

DC :-



$$R_{DC} = \frac{V_D}{I_D} = \frac{V_{D1}}{I_{D1}}$$

→ It is defined as the ratio of voltage across the diode to the current flowing through the diode.

AC :-

→ It is defined as the ratio of change in voltage to the change in current i.e.; $R_{ac} = \frac{1}{\frac{dI_D}{dV_D}} = \frac{1}{\text{slope}}$

$$R_{ac} = \frac{1}{\frac{dI_D}{dV_D}} = \frac{1}{I_0\left(e^{V_D/nV_T}\right) \times \frac{1}{nV_T}}$$

$$= \frac{nV_T}{I_0\left(e^{V_D/nV_T}\right)}$$

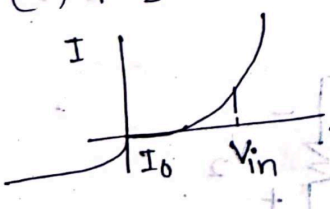
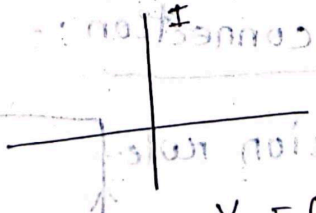
For forward bias, $I_D = I_0\left(e^{V_D/nV_T} - 1\right)$

$$\approx I_0\left(e^{V_D/nV_T}\right)$$

For reverse bias, $I_D = I_0\left(e^{V_D/nV_T} - 1\right)$

$$\approx I_0$$

Ideal diode Vs practical diode:

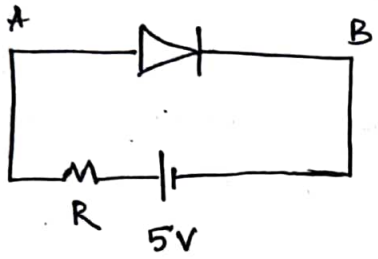
Practical	Ideal
(1) V-I 	
$V_{in} = 0.7$ V or 0.3V	$V_{in} = 0$V
(2) RB current $\neq 0$	0
(3) RB Resistance $\neq \infty$	$-\infty$

Equivalent model of PN Junction diode :-

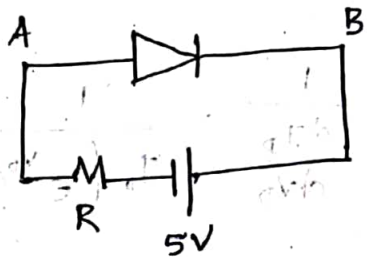
1. Linear peacewise mo
2. simplified model
3. Ideal model

→ check the diode is forward biased or reve biased and replace the diode by it's equiv model in any electric circuit.

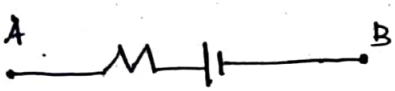
F.B



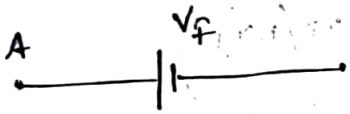
R.B



(1) Linear peacewise model :-



(2) simplified model :-



(3) Ideal model :-

Application :-

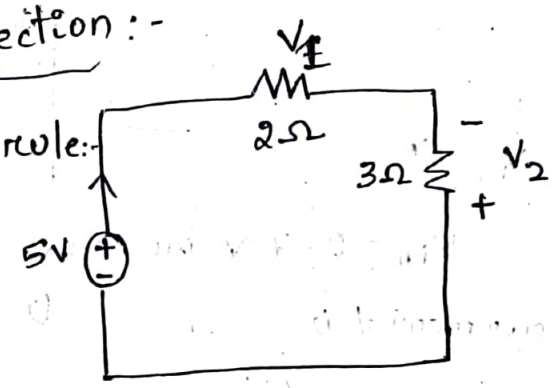
(1) Series diode connection :-

From

(a) voltage division rule :-

$$V_1 = \frac{V \times R_1}{R_1 + R_2}$$

$$V_2 = \frac{V \times R_2}{R_1 + R_2}$$

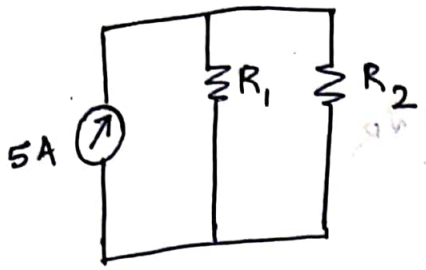


$V_1 = ?$, $V_2 = ?$

$$V_1 = \frac{5 \times 2}{2+3} = 2\,V$$

$$V_2 = \frac{-5 \times 3}{5} = -3\,V.$$

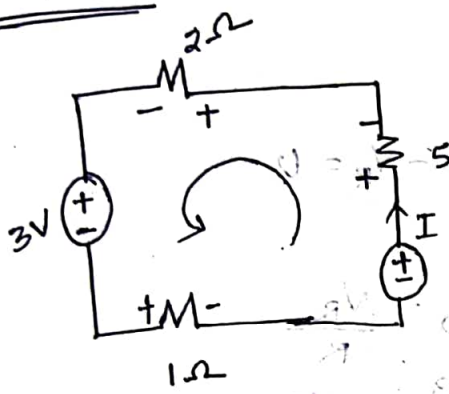
(b) Current division:-



$$I_1 = \frac{5 \times R_2}{R_1 + R_2}$$

$$I_2 = \frac{5 \times R_2}{R_1 + R_2}$$

(★) KVL :-



$$5 - 5I + 2I - 3 - I = 0$$

$$\Rightarrow 2 - 3I = 0$$

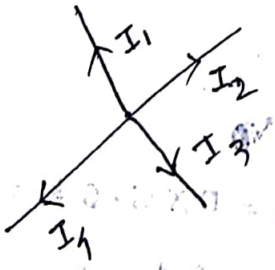
$$\Rightarrow I = \frac{1}{1}$$

statement:-

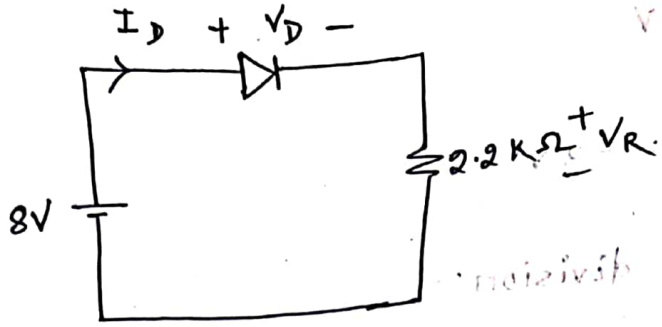
In a linear bilateral network, the algebraic sum of all voltage across a loop is zero (0).

(★) KCL :-

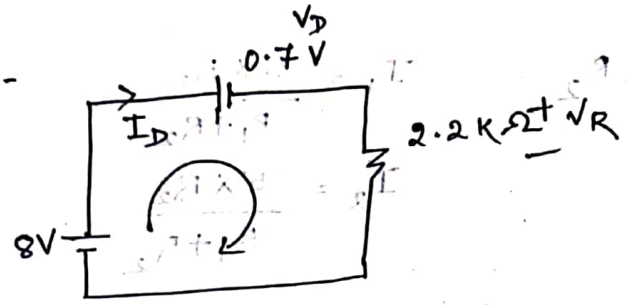
In a linear bilateral network, the algebraic sum of all current at any node is 0.



Q:- For the series diode connection shown in fig, determine V_D, V_R, I_D.



Soln :-



$V_D = 0.7\,V$

Applying KVL,

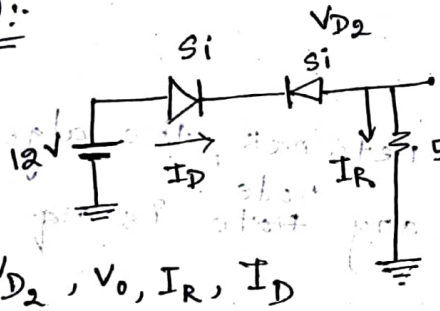
$$8 - 0.7 - V_R = 0$$

$$V_R = 7.3\,V$$

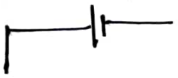
$$V_R = I_D \times 2.2\,K \Rightarrow I_D = \frac{V_R}{R}$$

$$\Rightarrow I_D = \frac{7.3}{2.2\,K\Omega} = \frac{73}{10 \times 22} \times 10 \times 10^3 = \frac{73}{22}\,KV$$

Q:-



V_{D_2}, V_0, I_R, I_D



$V_0 = 0 \times 5.6\,K = 0\,V$

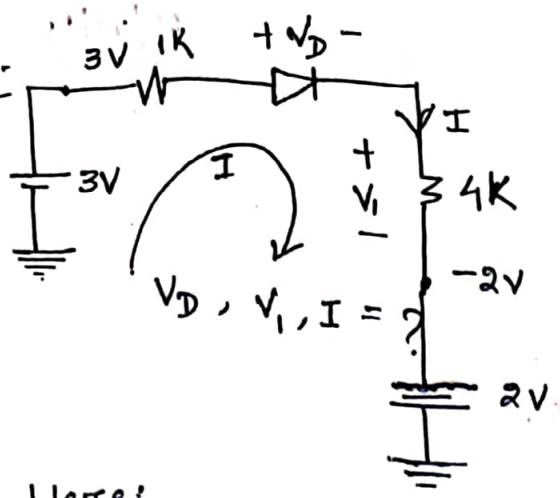
$I_R = 0\,A = I_D$

Applying KVL,

$$12 - 0.7 - V_{D_2} - 0 = 0$$

$$\boxed{V_{D_2} = 11.3\,V}$$

Q:-



Here;

$$3 - IXK - 4KI + 2 = 0$$

$$5KI = 5$$

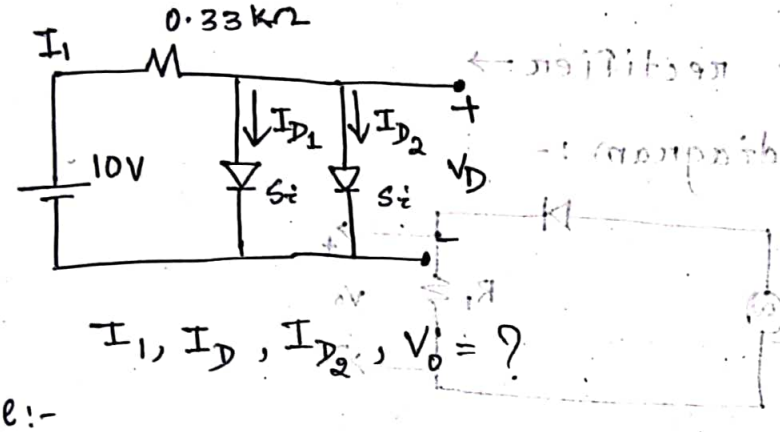
$$I = \frac{5}{5K} = 1\,mA$$

$$V_D = 0$$

$$V_1 = 4K \times 1mA$$

$$= 4V$$

Q:-

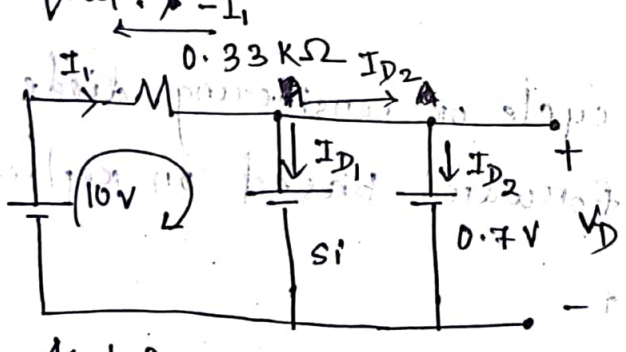


$I_1, I_D, I_{D_2}, V_0 = ?$

Note:-

→ Voltage across any two parallel ~~circuit~~ branches is always equal.

→ Current through 2 series element are always equal.



Applying KVL,

$$10 - 0.33K I_1 - 0.7 = 0$$

$$I_1 = \frac{9.3}{0.33}\,mA$$

$$V_0 = 0.7V$$

Applying KCL at A,

$$I_{D_1} + I_{D_2} + (-I_1) = 0$$

$$\Rightarrow 2I_{D_1} = I_1 \Rightarrow I_{D_1} = I_1/2$$

Application of diode :-

1. Diode as rectifier
2. Diode as clipper
3. Diode as clamper
4. Diode as switch .. etc.

→ Diode as Rectifier :-

Rectifier → It is an electronic circuit, which converts AC to DC. (Pulsating DC)

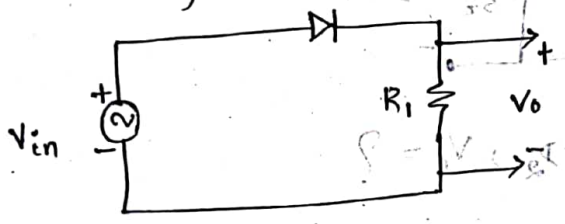
→ It is of 2 types.

(i) Half wave rectifier

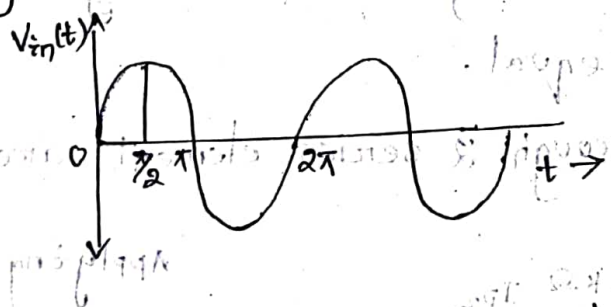
(ii) Full wave rectifier → Bridge type F.W.R
→ Center tapped F.W.R

Half wave rectifier →

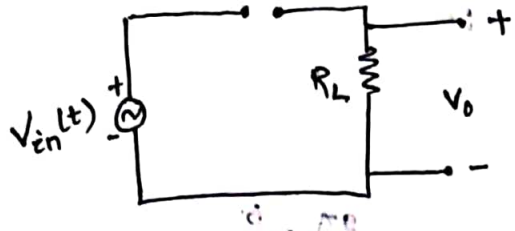
circuit diagram :-



Working Principle :-



→ During +ve half cycle on considering diode is ideal, diode is forward biased on replaced by short circuit.

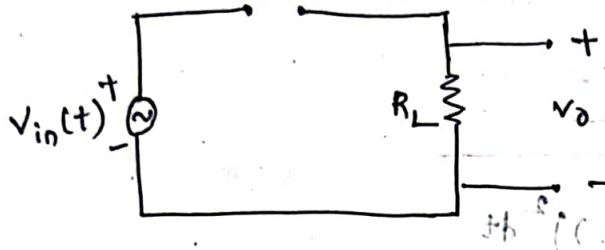


Apply KVL,

$$V_{in} - V_o = 0$$

$$\Rightarrow \boxed{V_{in} = V_o}$$

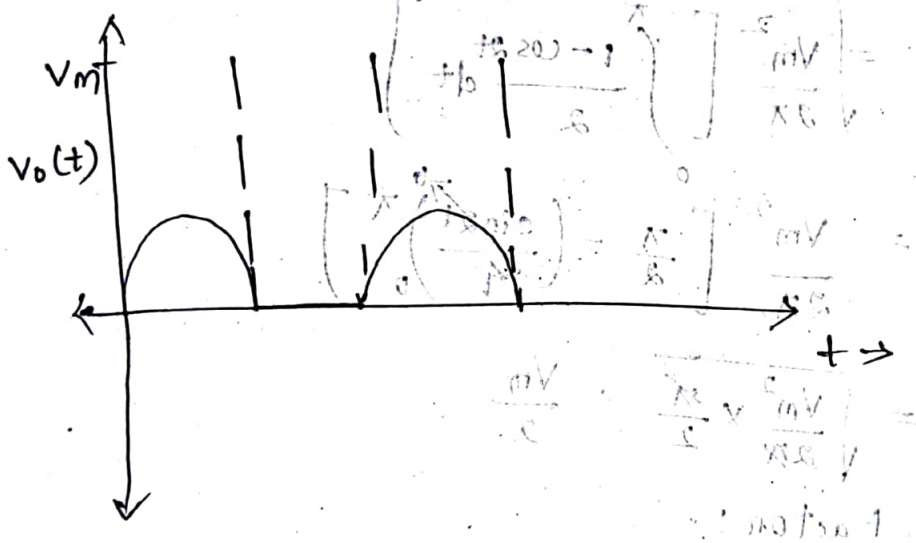
→ During -ve half cycle the diode will be ~~reverse~~ reverse based & replace the diode by open circuit.



Apply KVL,

$$V_o = 0 \times R_L$$

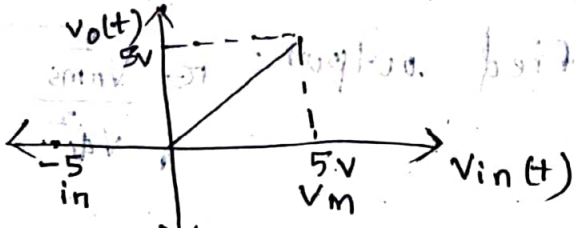
$$\Rightarrow \boxed{V_o = 0}$$



Transfer characteristics :-

~~→ When ever we will sketch time~~

→ the graph between input & output.



Calculation of $V_0(dc)$:-

$$V_0(dc) = \frac{1}{T_0}\int_0^{T_0} x(t)\,dt$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin t \cdot dt + \int_{\pi}^{2\pi} 0 \cdot dt\right]$$

$$= \frac{1}{2\pi}\left[V_m(-\cos t)\right]_0^{\pi}$$

$$= \frac{1}{2\pi} \cdot 2V_m$$

$$= \frac{V_m}{\pi}$$

V_0 (rms) calculation :-

$$V_0(rms) = \sqrt{\frac{1}{T_0}\int_0^{T_0} (x(t))^2\,dt}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} (V_m \sin t)^2\,dt + \int_{\pi}^{2\pi} 0}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\left[\int_0^{\pi} \frac{1-\cos 2t}{2}\,dt\right]}$$

$$= \frac{V_m^2}{2\pi}\left[\frac{\pi}{2} - \left(\frac{\sin 2t}{4}\right)_0^{\pi}\right]$$

$$= \sqrt{\frac{V_m^2}{2\pi} \times \frac{\pi}{2}} = \frac{V_m}{2}$$

Ripple Factor :-

→ A ripple factor is defined as the ratio of AC component present on output or half of the output to the DC component present in the rectified output :

$$r = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$= \sqrt{\frac{\left(\frac{V_m}{2}\right)^2}{\left(\frac{V_m}{\pi}\right)^2} - 1}$$

$$= \sqrt{\frac{V_m^2}{4} \times \frac{\pi^2}{V_m^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{4} - 1}$$

$$= 1.21$$

Efficiency of Rectifier :-

→ It is defined as the ratio of DC output power to the AC output power.

$$\eta = \frac{P_{dc(o/p)}}{P_{ac(o/p)}}$$

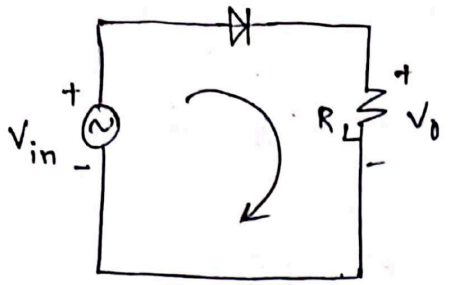
$$= \frac{\frac{V_{dc}^2}{R_L}}{\frac{V_{rms}^2}{R_L}}$$

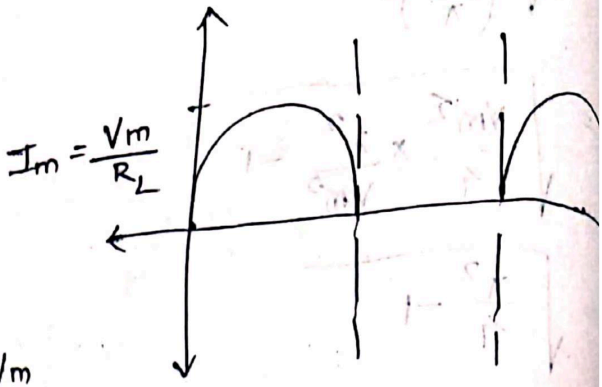
$$= \frac{V_{dc}^2}{V_{rms}^2}$$

$$= \frac{\left(\frac{V_m}{\pi}\right)^2}{\left(\frac{V_m}{2}\right)^2}$$

$$= 40.6\%.$$

09/09/19





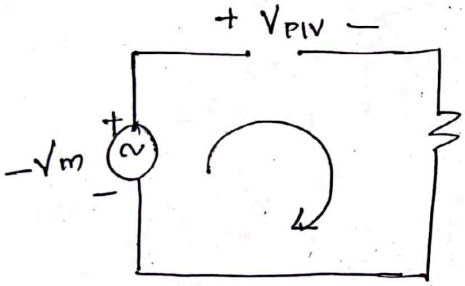
$$I_{rms} = \frac{I_m}{2} = \frac{\frac{V_m}{R_L}}{2} = \frac{V_m}{2R_L}$$

$$V_{dc} = V_{avg} = \frac{V_m}{\pi}$$

$$I_{dc} = I_{avg} = \frac{I_m}{\pi} = \frac{\frac{V_m}{R_L}}{\pi} = \frac{V_m}{\pi R_L}$$

~~Peak reverse bias~~ Peak Inverse Voltage:- (Calculation of PIV)

→ It is defined as the apply peak reverse bias voltage applied across the diode such that diode will safely work. (or diode will not work)



$$(-V_m) - V_{PIV} = 0$$

$$\Rightarrow \boxed{V_{PIV} = -V_m}$$

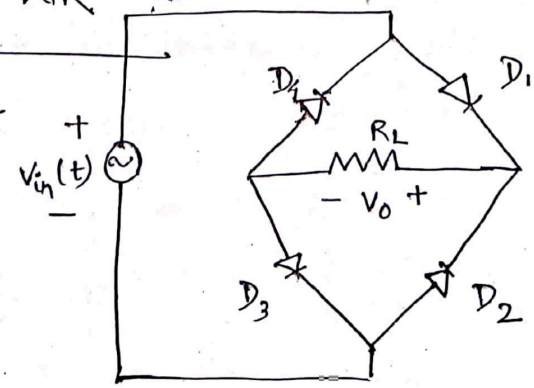
$$V_{PIV} = |-V_m| = V_m$$

$$\boxed{V_{PIV} \leq V_m}$$

(1)

Bridge type FWR :-

Circuit diagram-



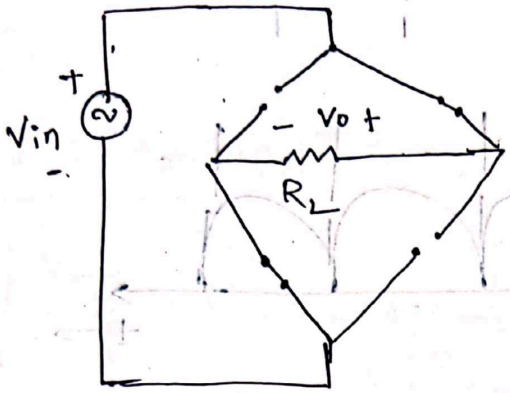
Operation :-

→ During +ve half cycle D_1 & D_3 - forward biased
D_2 & D_4 - Reverse biased.

D_1 & D_3 will be replace by short circuit.

D_2 & D_4 " " " " open circuit.

→ And circuit become now :-



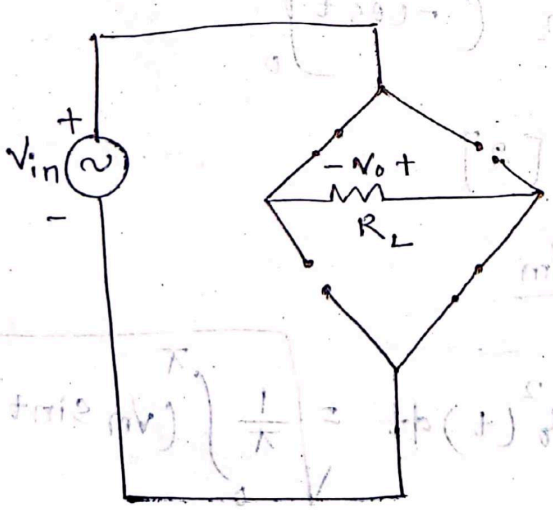
Applying KVL,

$$V_{in} - V_o = 0$$

$$\Rightarrow \boxed{V_{in} = V_o}$$

→ During -ve half cycle, D_1 & D_3 will be reverse biased & replaced by open circuit.

And D_2 & D_4 - forward biased - replace by short circuit.



$$V_{in} + V_o = 0$$

$$\boxed{V_{in} = V_o}$$

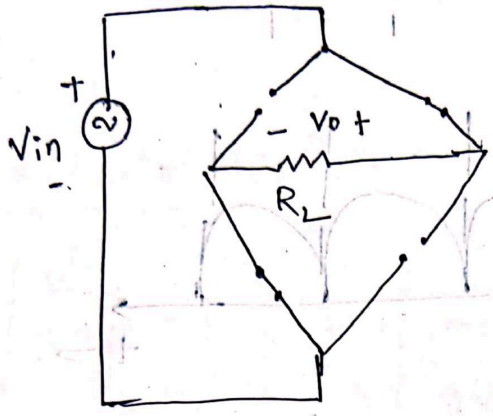
Operation :-

→ During +ve half cycle D_1 & D_3 - forward biased
D_2 & D_4 - Reverse biased.

D_1 & D_3 will be replace by short circuit.

D_2 & D_4 " " " " open circuit.

→ And circuit become now :-



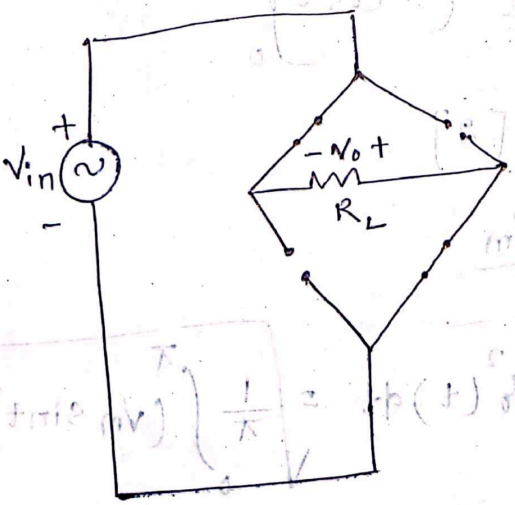
Applying KVL,

$$V_{in} - V_o = 0$$

$$\Rightarrow \boxed{V_{in} = V_o}$$

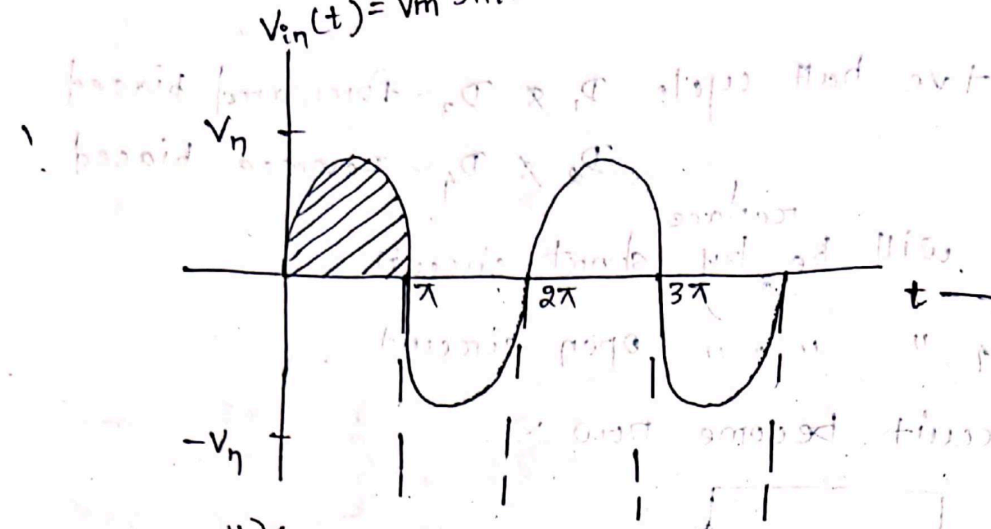
→ During -ve half cycle, D_1 & D_3 will be reverse biased & replaced by open circuit.

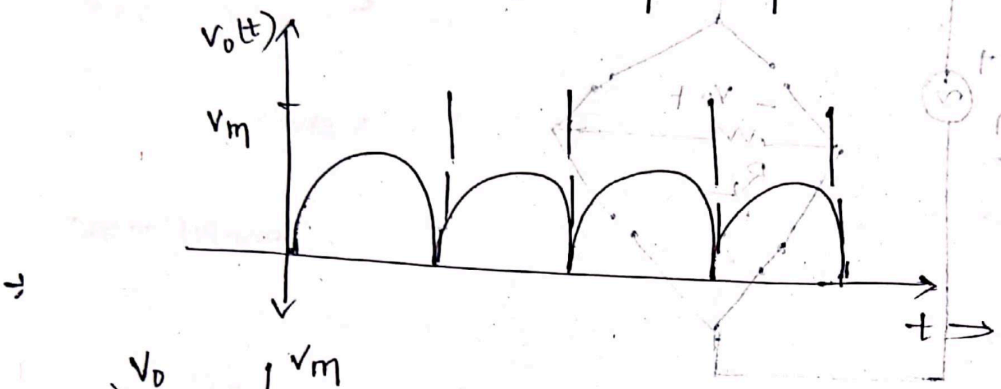
And D_2 & D_4 - forward biased - replace by short circuit.

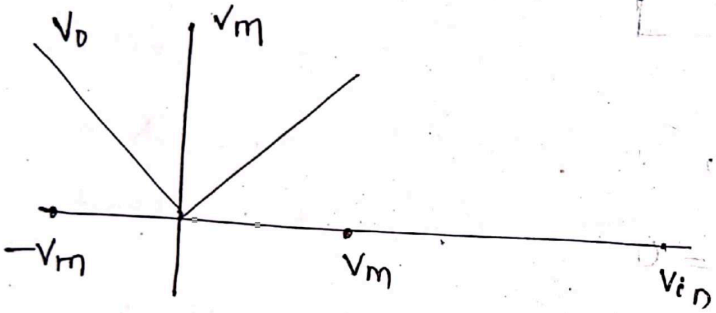


$$V_{in} + V_o = 0$$

$$\boxed{V_{in} = V_o}$$







$$V_{dc(o)} = V_{avg(o)} = \frac{1}{T_o} \int_{\langle T_o \rangle} V_o(t)\, dt$$

$$= \frac{1}{\pi} \int_0^{\pi} V_m \sin t \cdot dt$$

$$= \frac{V_m}{\pi} \left[-\cos t \right]_0^{\pi}$$

$$= \frac{V_m}{\pi} [2]$$

$$\therefore \frac{2V_m}{\pi}$$

$$V_{rms(o)} = \sqrt{\frac{1}{T_o} \int_0^{T_o} V_o^2(t)\, dt} = \sqrt{\frac{1}{\pi} \int_0^{\pi} (V_m \sin t)\, dt}$$

$$= \sqrt{\frac{V_m^2}{\pi} \int_0^{\pi} \frac{1-\cos 2\theta}{2}\, dt}$$

$$= \sqrt{\frac{V_m^2}{\pi} \left(\frac{t}{2} - \frac{\sin 2t}{4}\right)_0^{\pi}}$$

$$= \sqrt{\frac{V_m^2}{\pi} \left(\frac{\pi}{2} - \right)}$$

$$= \frac{V_m}{\sqrt{2}}$$

Ripple factore Cal^n :-

$$\pi = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1} = \sqrt{\frac{\frac{V_m^2}{2}}{\frac{4V_m^2}{\pi^2}} - 1}$$

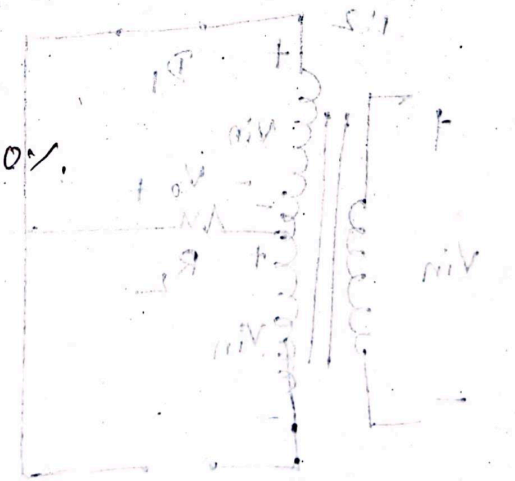
$$= \sqrt{\frac{\pi^2}{8} - 1} \quad = 0.482$$

Efficiency :-

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\ \%$$

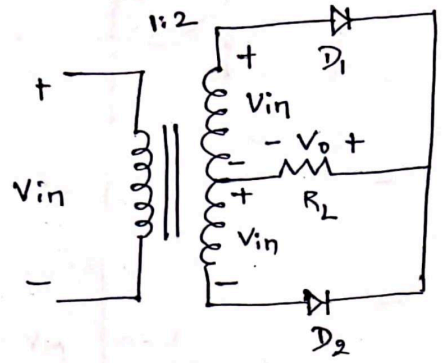
$$= \frac{\frac{V_{dc}^2}{R_L}}{\frac{V_{ac}^2}{R_L}} \times 100\%$$

$$= 81\%$$



(2) Centere tapped type FWR.

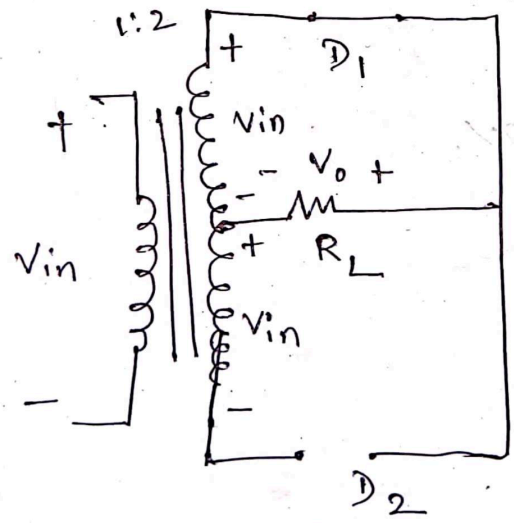
Circuit diagram :-



Operation :-

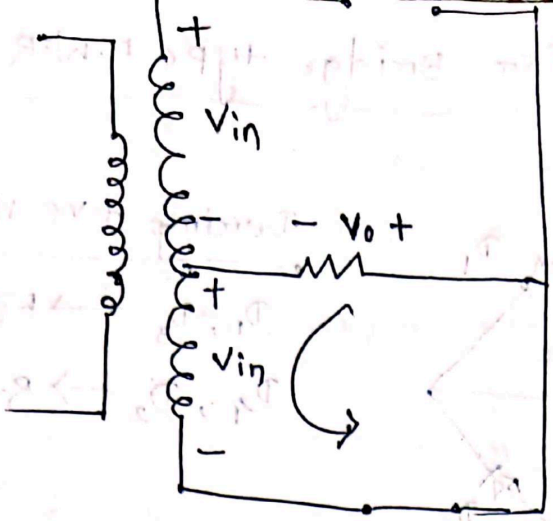
→ The turn ratio of the transistor is 1:2. So, voltage appear across the secondary coil is 2Vm.

→ During +ve half cycle of Vin,
D1 will be forward biased, replace by short circuit.
D2 " reverse ", replace by open circuit.



Applying KVL,
$-V_o + V_{in} = 0$
$\Rightarrow V_o = V_{in}$.

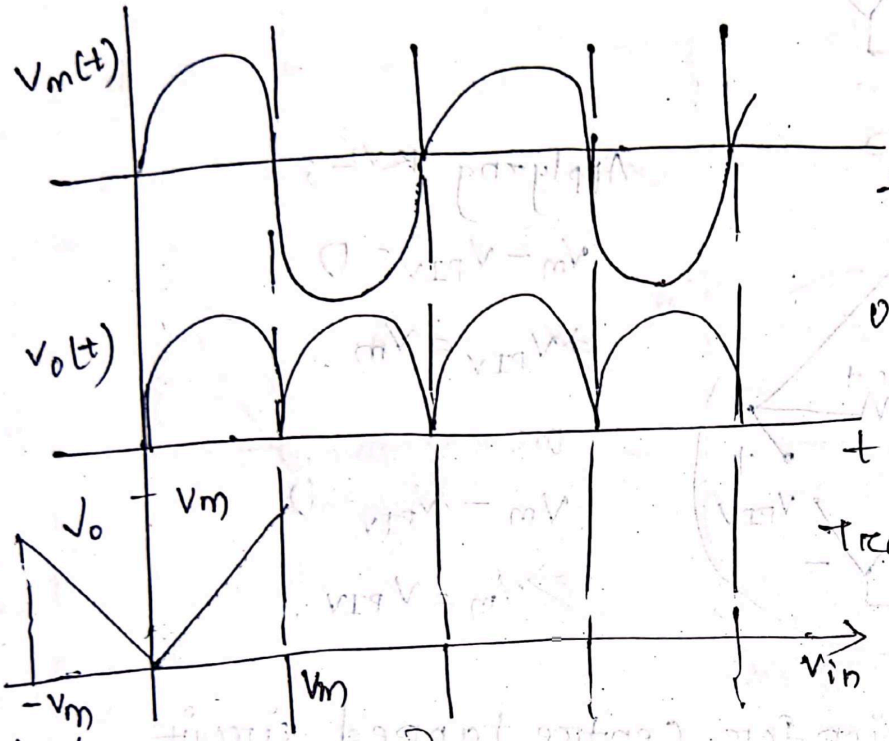
→ During −ve half cycle of Vin,
D1 is reverse biased.
D2 is forward biased.



Applying KVL :-

$-V_o - V_{in} = 0$

$\Rightarrow \boxed{V_o = -V_{in}}$



Input chare.

OUTPUT chare..

Transfere chare.

→ V_{dc} →

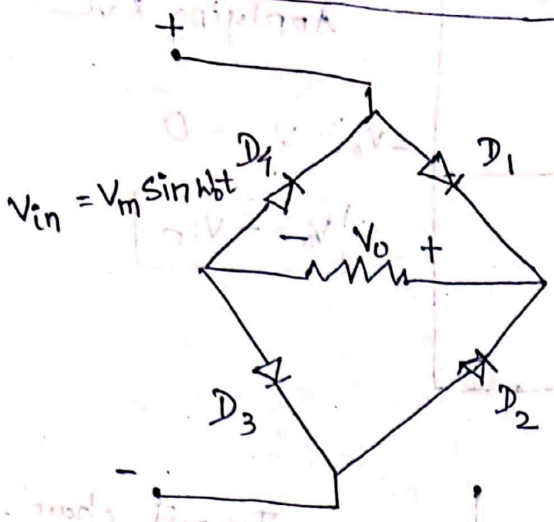
Repel factore →

V_{rms} →

Efficiency

} Same as bridge type rectifer

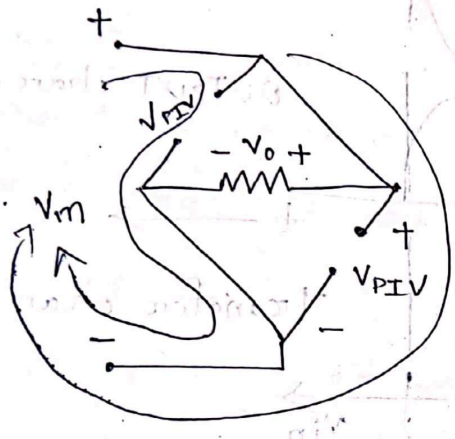
PIV Calculation for Bridge type F.W.R :-



∴ During +ve HC :-

$D_1, D_3 \rightarrow$ F.B

$D_4, D_2 \rightarrow$ R.B



Applying KVL;

$V_m - V_{PIV} = 0$

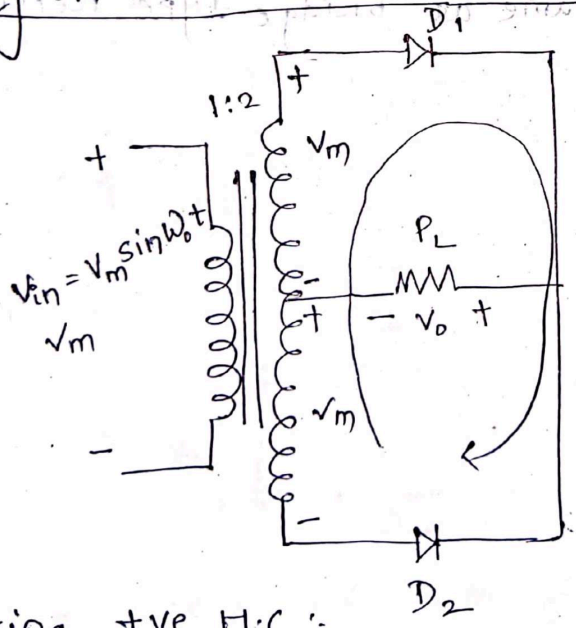
$\Rightarrow V_{PIV} = V_m$.

or

$V_m - V_{PIV} = 0$

$\Rightarrow V_m = V_{PIV}$.

PIV Calculation for Centre tapped circuit diagram :-



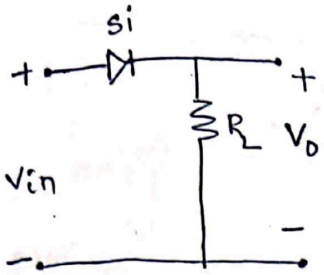
During +ve H.C :-

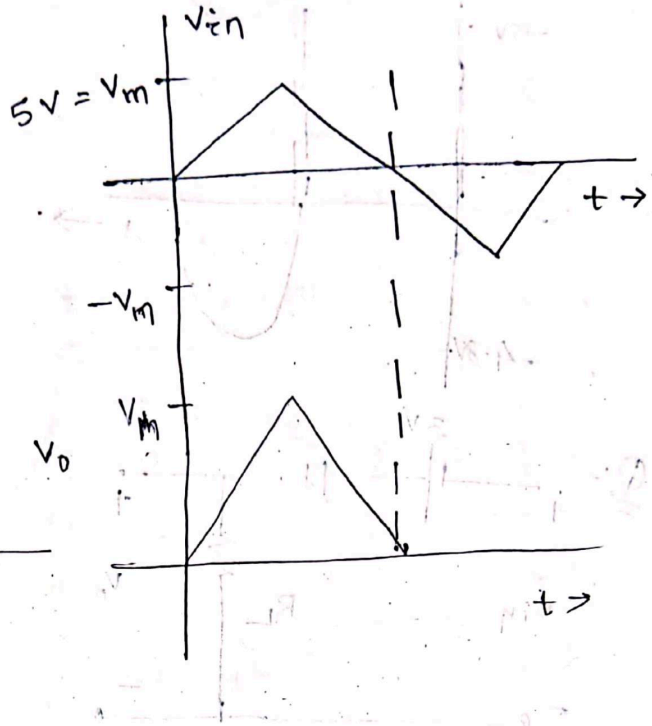
Applying KVL; $V_{PIV} + V_m + V_m = 0$

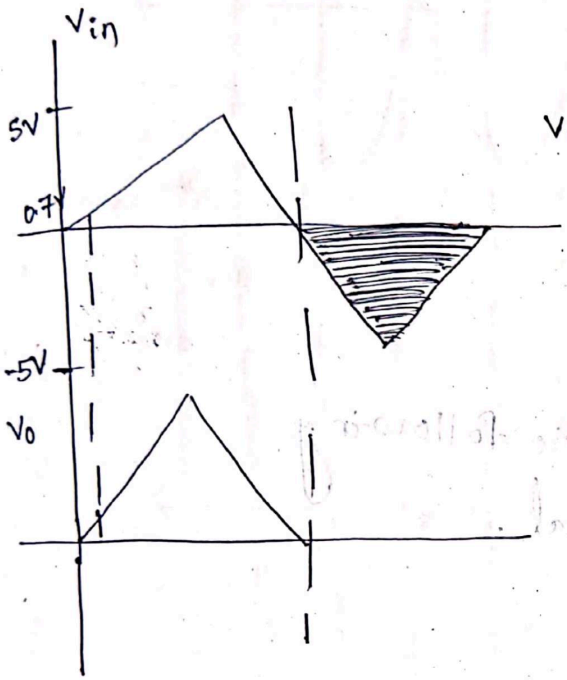
$\Rightarrow V_{PIV} = |-2V_m| = 2V_m$.

✓ Clipper:-

→ It is an electronic circuit consisting of diode, resistor; which is used to click or remove some portion of apply input signal.



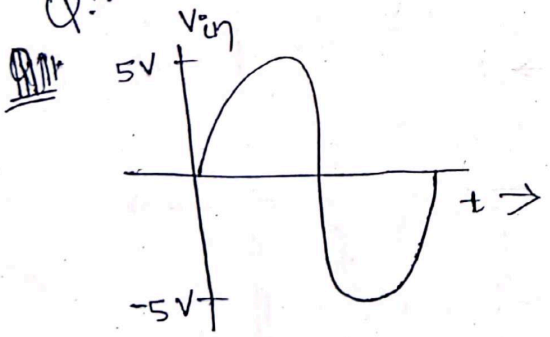


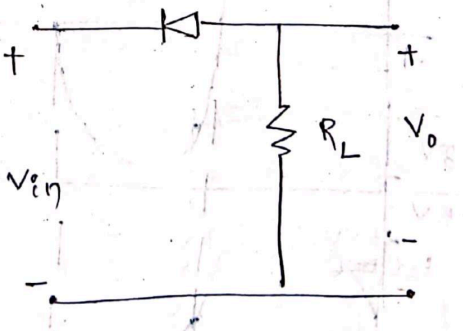


$V_o + 0.7 - 1.3 = 0$

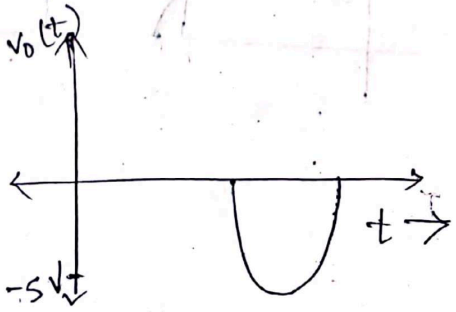
$\Rightarrow \boxed{V_o = 1.6}$

Q:-

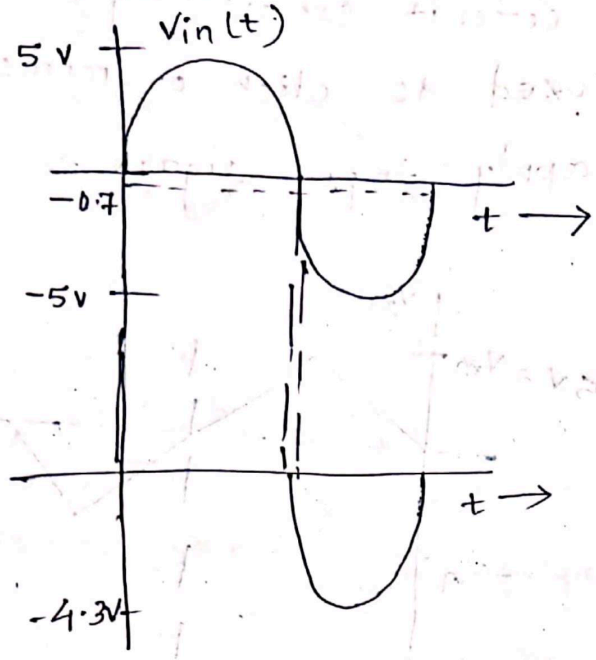




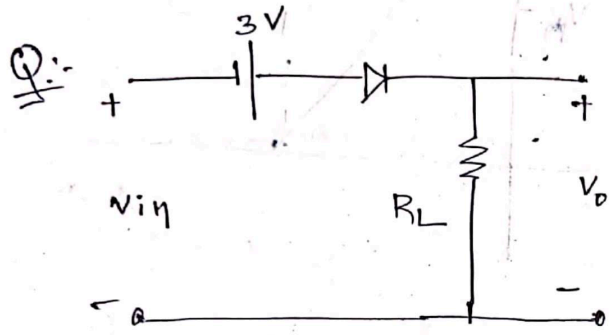
Here; for ideal diode



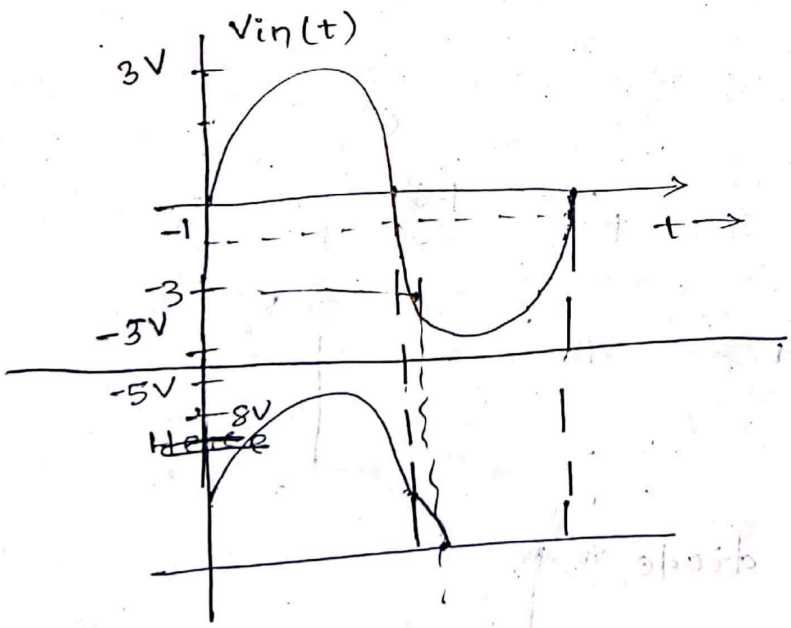
$V = 0.7V$ (Non-ideal)

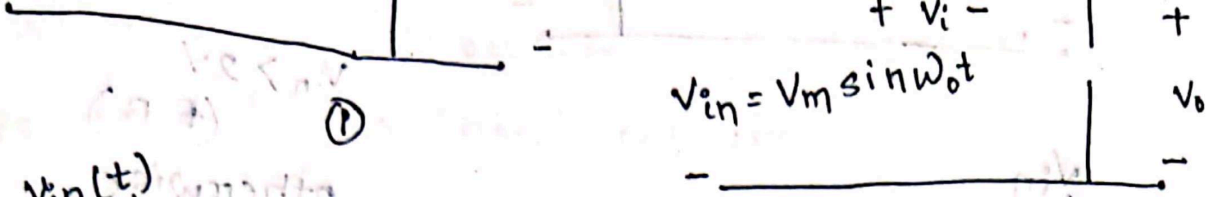


Q:-



Sketch the output of the following concide the diode is ideal.

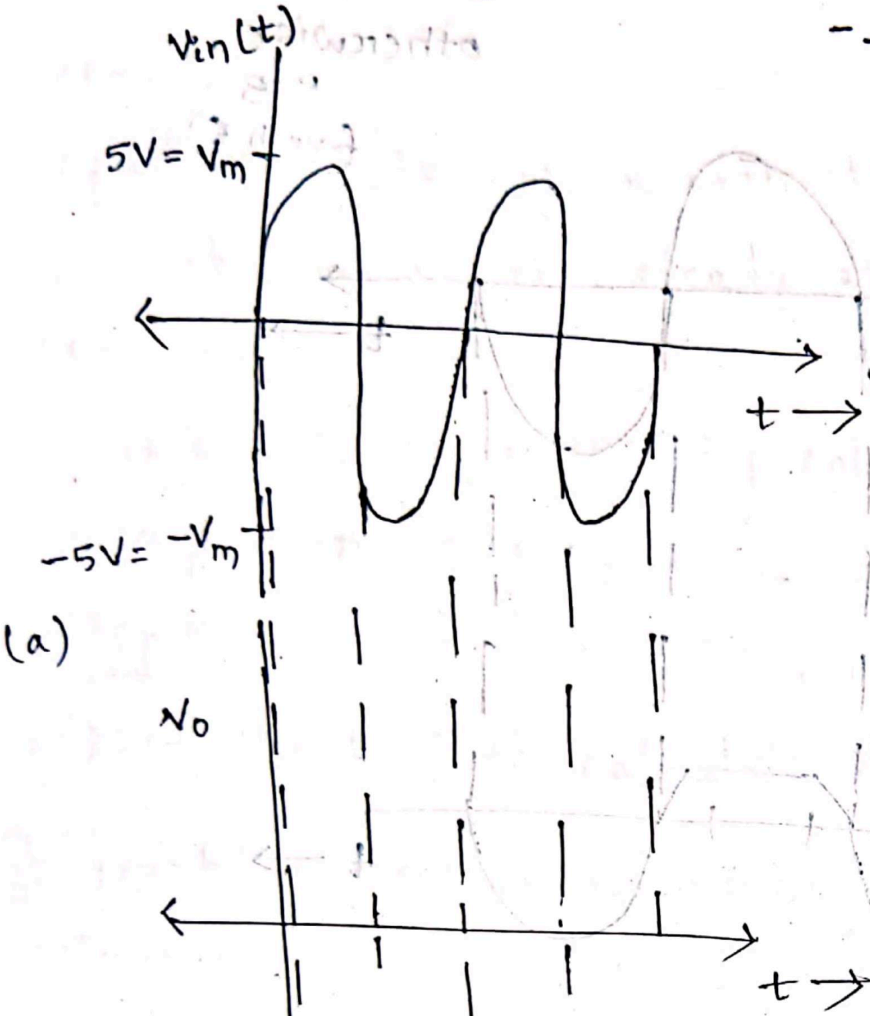




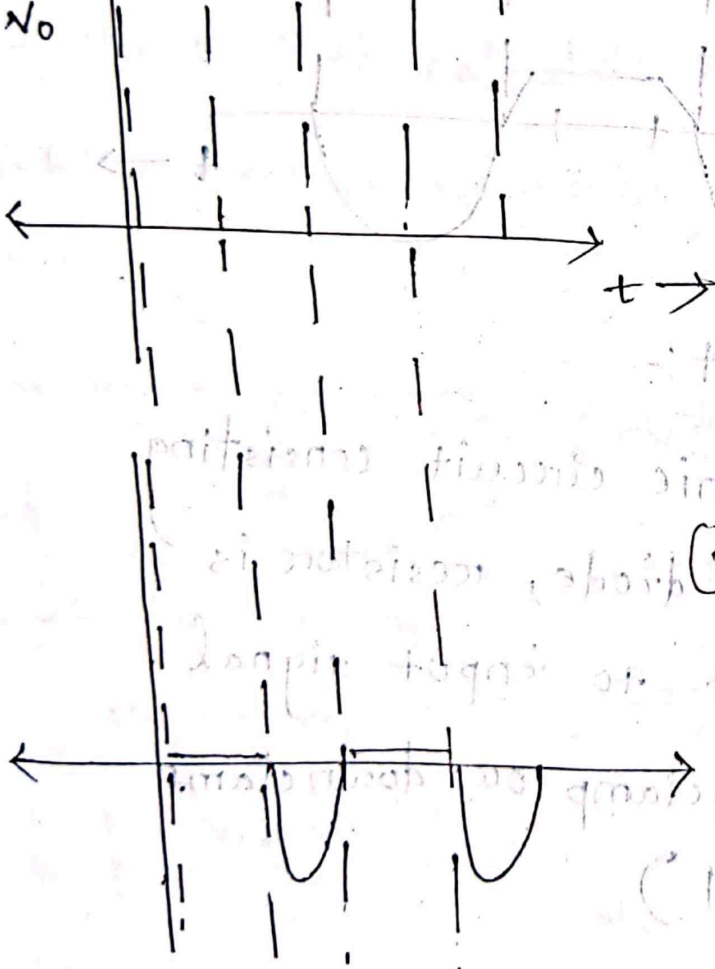
$v_{in} = V_m \sin \omega_o t$

①

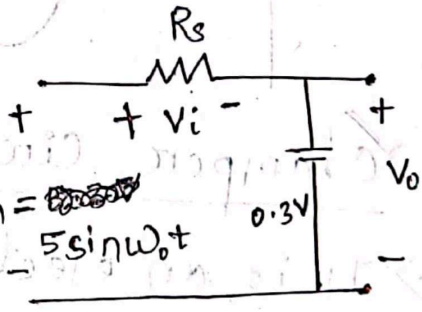
②



(a)



(b)



$v_{in} = 5 \sin \omega_o t$

③

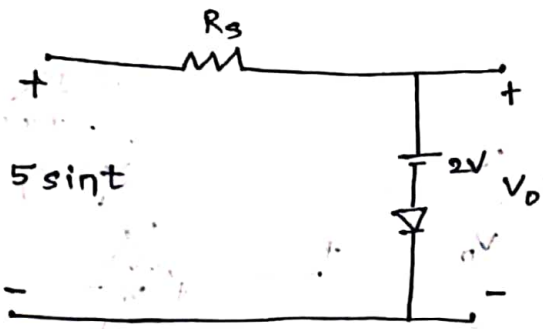
③

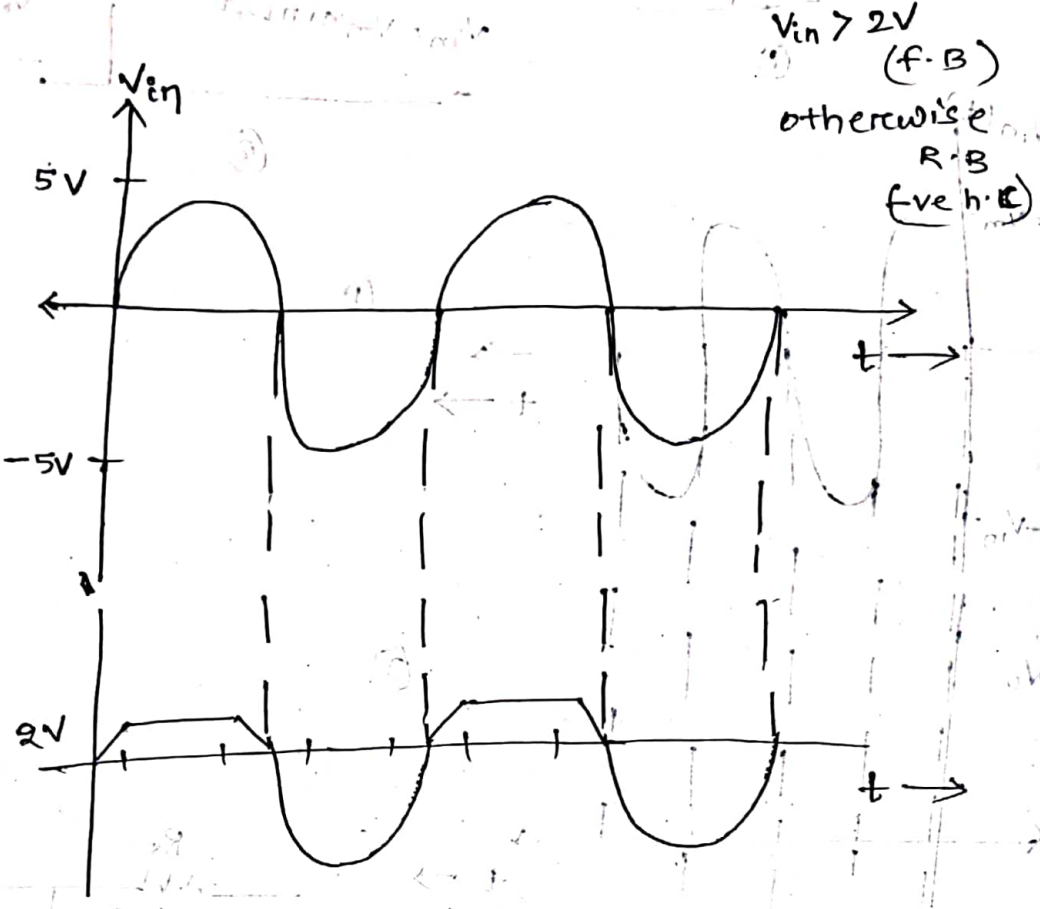
$V_o - 0.3V = 0$

$\Rightarrow V_o = 0.3V$.

Parcallel branch
= Voltage equal.

Q:-2



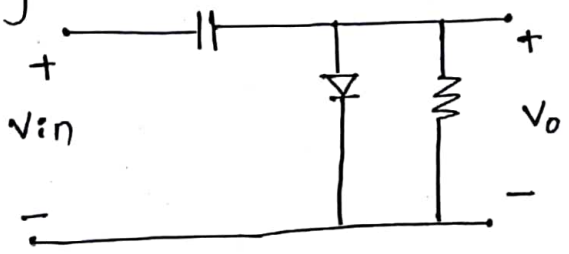


Clamper Circuit:-

→ It is an electronic circuit consisting of capacitance, diode, resistor is used for add dc to input signal.

- (It can be upclamp or downclamp the input signal)

Circuit diagram:-



Steps / Procedure to analysis the clamper circuit:-

Step-1 :-

Start the analysis of clamper circuit from that part of half cycle of input such that the diode will be forward bias & replace the diode with by a short circuit.

Step-2 :-

Capacitor will get a path to charge & it will charge to its steady state voltage.

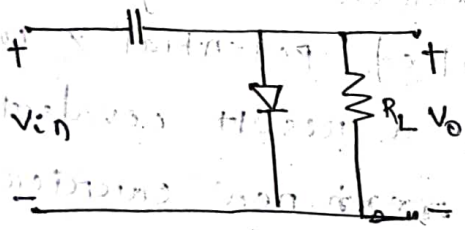
Step-3 :-

Replace the capacitor by calculated steady state voltage from step 2.

Step-4 :-

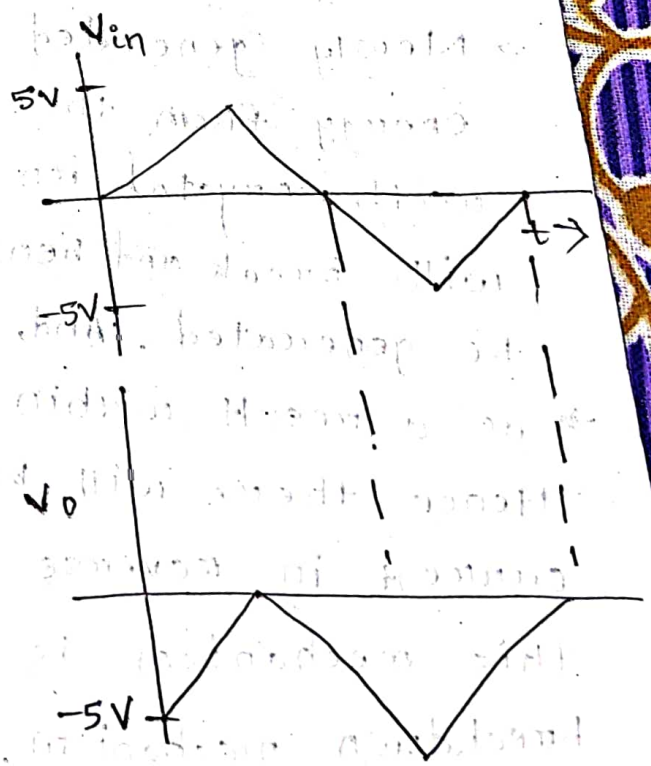
Apply the KVL to calculate the output voltage (V_o)

Q. Sketch the output waveform from the following circuit :-



$$V_{in} - 5 - V_o = 0$$

$$\Rightarrow \boxed{V_o = V_{in} - 5}$$

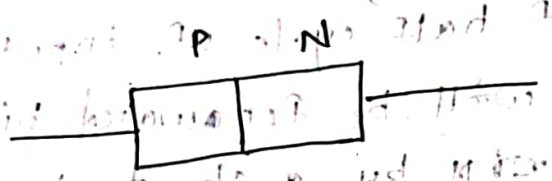


18/09/19

Zener diode:-

→ It is heavily dopped P-N junction diode.

→ Construction wise both are same, only difference in dopping conc.



V-I characteristics:-

→ V-I characteristics of zener diode consists up 2 parts. 1) Forward biased (same as F.b of normal P-N junction diode)

2) Reverse biased

It is divied into 2 parts:-

(a) Non-breakdown (same as normal P-N junction diode)

(b) Breakdown Mechanism:-

→ A thermally generated carrier falls down in junction diode, which will collide with crystal ion, as a result covalent bond is break, & hence carriers will generated.

→ Newly generated carrier will get sufficient energy from the applied potential & collide with crystal ion as a result covalent bond will break and hence new carrier will be generated. And, the same process continue, as a result within some times, a large no. of carrier will generated

→ Hence there will be sharp raise in current in reverse biased.

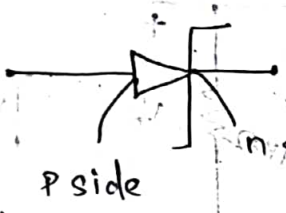
this mechanism is known as Avalanche breakdown mechanism.

Zener break down:-

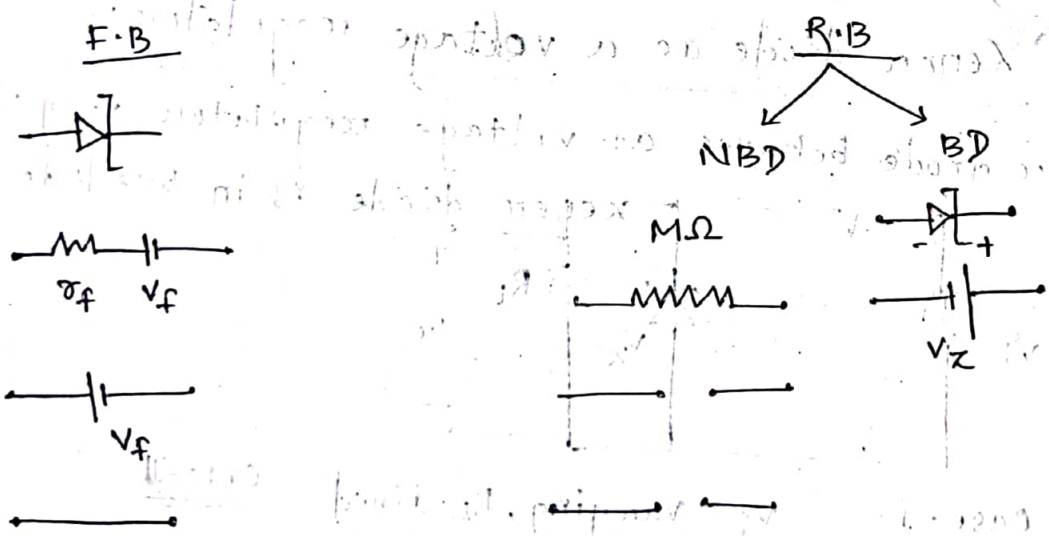
→ Due to heavily dopped P-N junction, a high electric field will be at the junction; due to this high electric field a large amount of force will be on the carrier. This large force will pull out carrier from the covalent bond of the crystal bond. Also newly generated carrier will have high force & they will pull out carriers from the covalent bond. As a result, large no. of carrier and hence there is short raise in current.

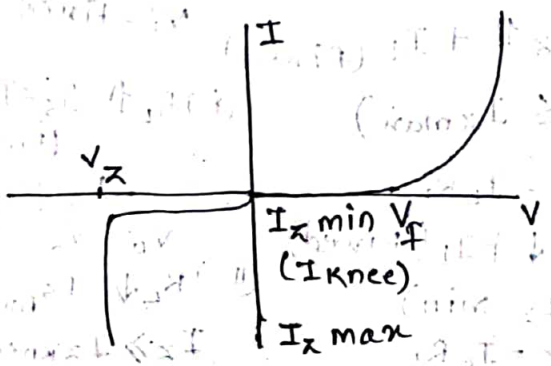
this is called zener break down mechanism.

Schematic diagram of zener diode:-



Equivalent model of zener diode:-



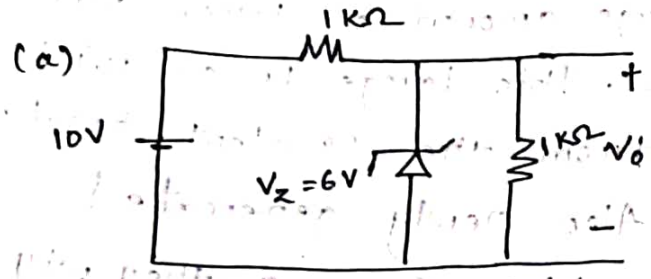


Application :-

→ It behaves as voltage regulator.

Q. Calculate V_o for the following circuit.

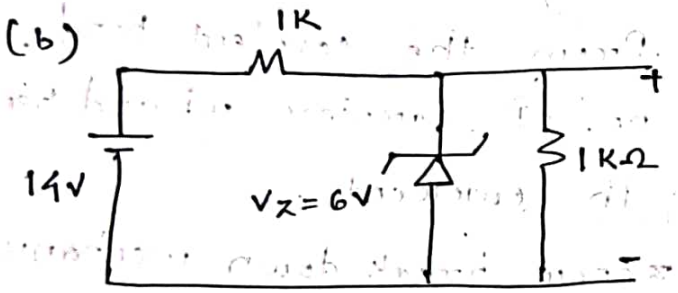
(a)



$$V_o = \frac{10 \times 1K}{1K+1K} = 5V$$

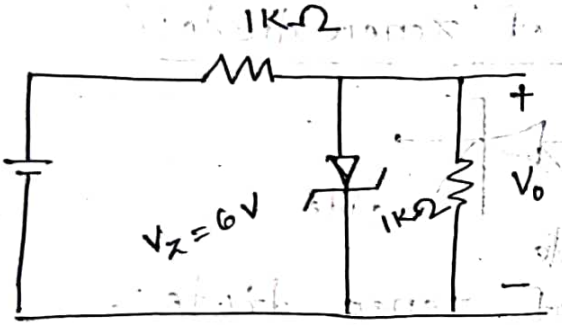
$\Rightarrow \boxed{V_o = 5V}$

(b)



$\boxed{V_o = 6V}$

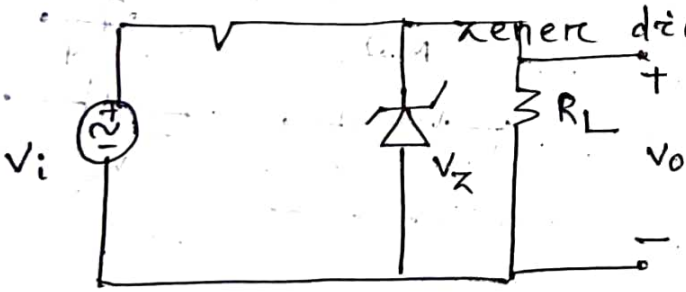
(c)



$\boxed{V_o = 0V}$

Zener diode as a voltage regulator :-

Zener diode behaves as voltage regulator only when zener diode is in breakdown.



Case-I V_i = Varying, R_L = fixed

(i) $V_i \uparrow$ $I_{SP} = I_Z \uparrow + I_L$ (fixed)

$(I_Z \leq I_{Z\max})$

$V_o = V_Z = I_L R_L$

(ii) $V_i \downarrow$ $I_S \downarrow = I_Z \downarrow + I_L$ (Fixed)

$(I_Z \geq I_{Z\min})$

$V_o = V_Z = I_L R_L$

Case-II V_i = fixed R_L = Varying

(i) $R_L \uparrow$ $I_S = I_Z \uparrow + I_L \uparrow$ (fixed)

$I_Z < I_{Z\max}$

$V_o = V_Z = I_L \downarrow R_L \uparrow$

(ii) $R_L \downarrow$ $I_{S_{fixed}} = I_Z \downarrow + I_L \uparrow R$