17/10/19

Unit-III Field effect Transistor (FET)

FET is a three terminal device (Gate (G), Source (S), Drain (D)) in which o/p current (I_D) for each control by i/p voltage (V_{GS}).

V_{GS} = Voltage bet^n G & S.

$$I_D = f(V_{GS})$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

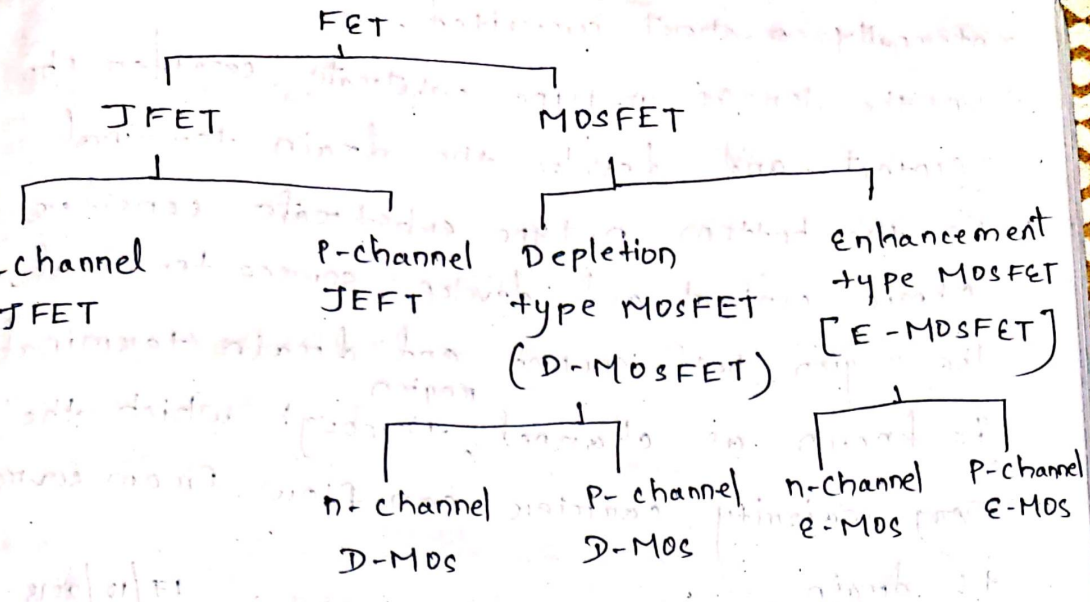
Difference bet^n BJT & FET:-

BJT	FET
1. BJT is current control current source device.	1. FET is voltage control current source device.
2. I/p impedance of BJT is small as compare to FET. (Range is kΩ)	2. The i/p impedance of FET is very large. (Range is MΩ)
3. O/p impedance is large in compare to FET.	3. O/p impedance is less
4. It is the bipolare device bcoz conduction is due to both polarity charactere. i.e; majority & minority charactere.	4. It is Unipolare device bcoz conduction is due to only the majority charactere.

⇒ FET Tree:-

→ It is Based on the isolation bet^n gate and channel FETs are classified as follows.

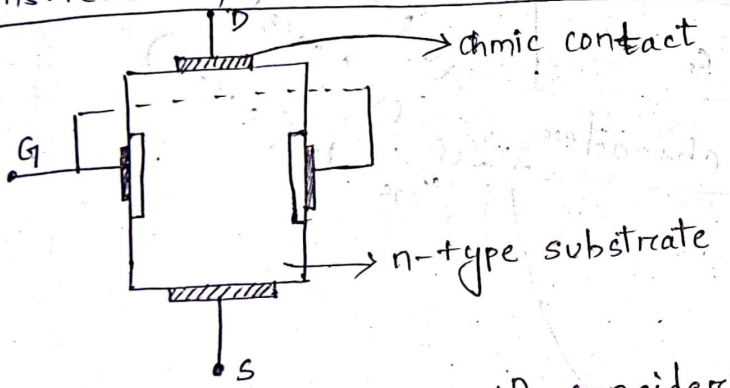
It is of 2 types.



JFET :-

When the isolation bet^n Gate & channel is done by P-N junction. that class of FET is known as Junction filled effect transistor.

Construction of n-channel JFET :-



→ For n-channel JFET const^n consider a lightly dopped n-type material (n-type substrate) embeded two heavily dopped p-type material on 2 sides of n-type substrate. As a result, there will be P-N junction bet^n p-type & N-type material.

→ On the p-type material consider ohmic contact and develop gate terminal.

→ On both sides of n-substrate Gate terminals are

internally a short circuited.

→ On the top of n-type substrate consider ohmic contact and develop the drain terminal.

→ On the bottom n-type substrate consider ohmic contact and develop source terminal.

→ The region bet^n source and drain terminal is known as channel region through which the majority carriers can flow from source to drain.

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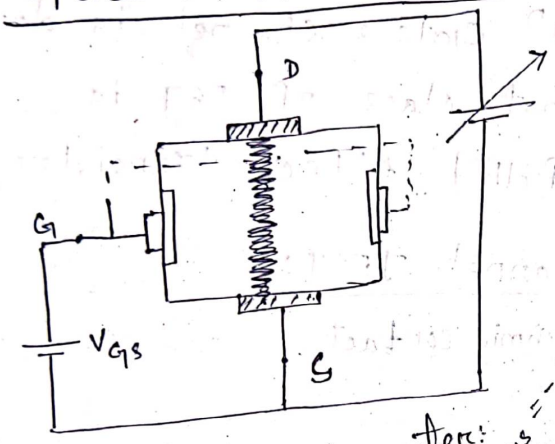
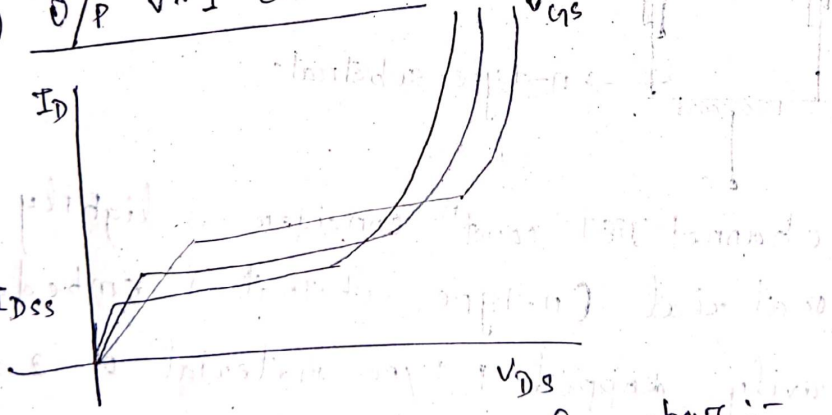
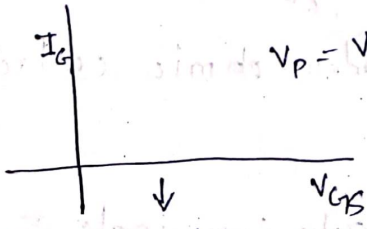
Operation of n-channel JFET :-



(1) O/P V-I characteristics:

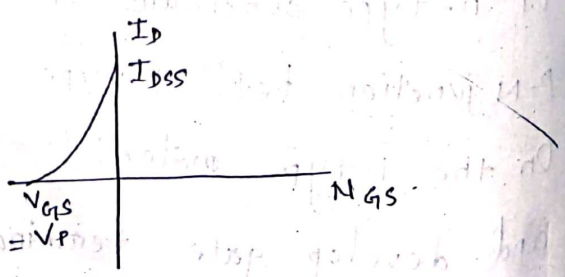


(2) I/P :-



very less amount of I_G will flow $\cong 0A$.

Transfer char :-



Case-1

→ Considering $V_{GS} = 0V$, as increasing V_{GS} +vely.

→ A more no. of carrier will flow from source towards drain. As a result I_D (electron current) will flow from drain towards source.

→ During application of V_{DS} +vely, the P-N junction will be reversebias, the reverse-bias effect across the junction will increase from bottom towards top.

So, depletion region will be "wedge shape".

(This is bcoz the entire s.c device behaves as resistor from source to drain & entire V_{DS} will be drop across the resistor, and this voltage drop will be increase from source towards drain.

And hence, the reverse biased effect will increase from source towards drain.

As a result deption region will be "wedge shape".)

→ If we further increase V_{DS}, I_D current gets saturated, and if we increase V_{DS} further the I_D current is constant, bcoz channel is fixed, if we further increase the V_{DS}, then the sharp raise in I_D current bcoz of break down.

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Pinch-off current :-

→ The value of V_{ds}, at which I_D current gets constant, then pinch-off occurs.

→ The value of V_{GS} at which $I_D = 0$, is also known as pinch-off currents.

→ The value of V_{GS} at which $I_D = 0$, that value of V_{GS} is known as pinch-off voltage.

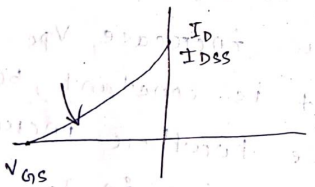
i) For n-channel ~~JFET~~ JFET, pinch-off voltage JFET = -ve.

ii) For p-channel JFET, pinch-off voltage JFET is +ve.

Transfer char :-

~~While increasi~~

For n-channel JFET, by increasing the value of JFET, I_D current gets reduce & pinch-off voltage $V_{GS} = V_P$, $I_D = 0$.



The eqn best fit for above transfer characteristics is developed by circuit & is known as schokelay.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \rightarrow \text{schokelay eqn}$$

Derivation of Transconductance (g_m) :-

→ Transconductance is defined as the ratio of o/p current to the input voltage. i.e; change in I_D / change in V_{GS}. $\boxed{g_m = \frac{I}{V}}$

$$\Rightarrow \boxed{g_m = \frac{\partial I_D}{\partial V_{GS}}}$$

$$\Rightarrow \boxed{g_m = \frac{dI_D}{dV_{GS}}}$$

$$\frac{dg_m}{dV_{GS}} = \frac{d^2 I_D}{d^2 V_{GS}} \quad \frac{dV_{GS}(d^2 I_D) + dI_D(dV_{GS})}{(dV_{GS})^2}$$

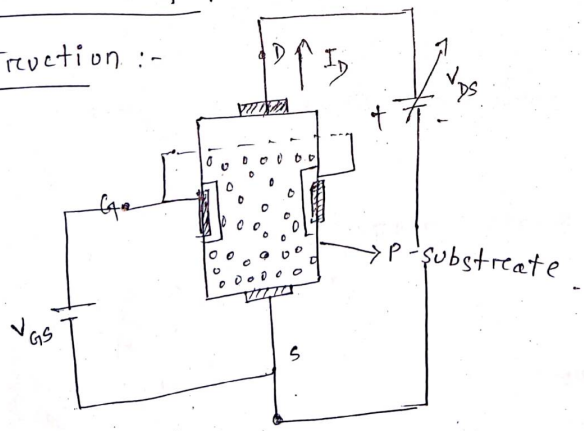
$$= \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \right]$$

$$= I_{DSS} \times \frac{1}{-V_P} \times 2\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$\boxed{g_m = -\frac{2 I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] \text{ ohm}^{-1} \text{ or } \Omega^{-1} \text{ or mho}.}$$

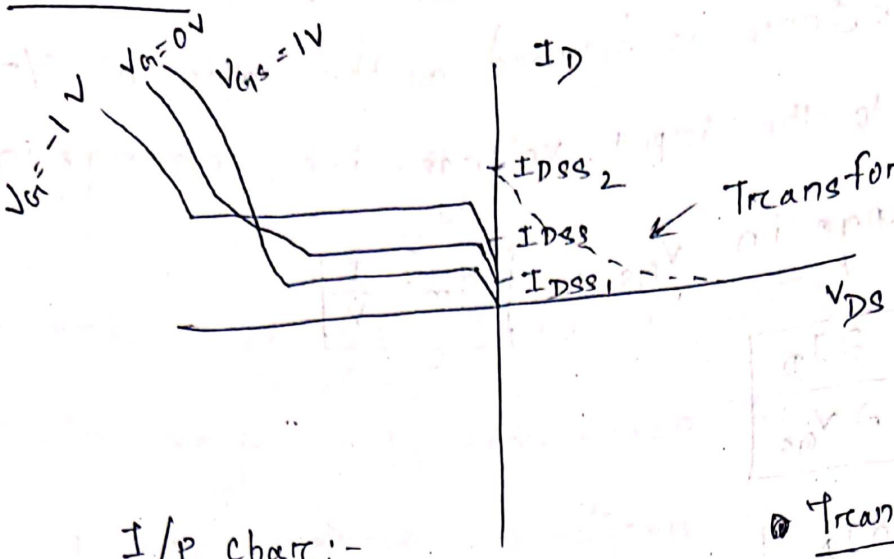
P-channel JFET :-

construction :-

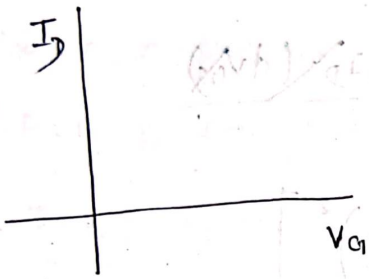


Operation :-

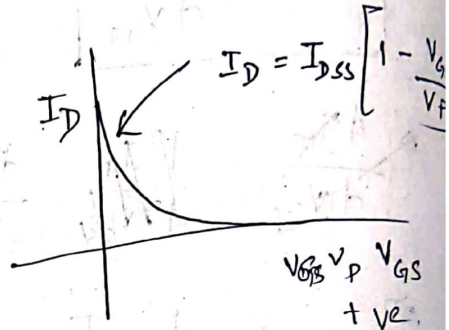
$V_{GS} = 0.V$



I/P char :-



• Transfer char :-

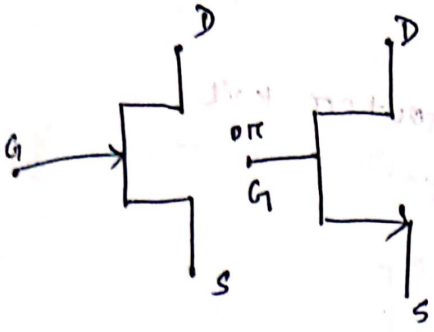


$$g_m = \frac{\partial I_D}{\partial V_{GS}} = -2\,\frac{I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right].$$

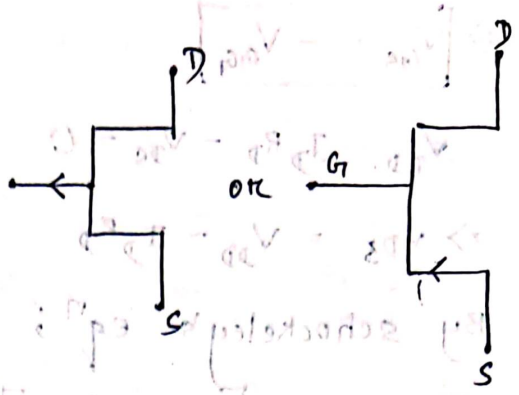
Symbol / Schematic diagram of JFET :-

23/10/19

n-channel JFET :-



P-channel JFET :-

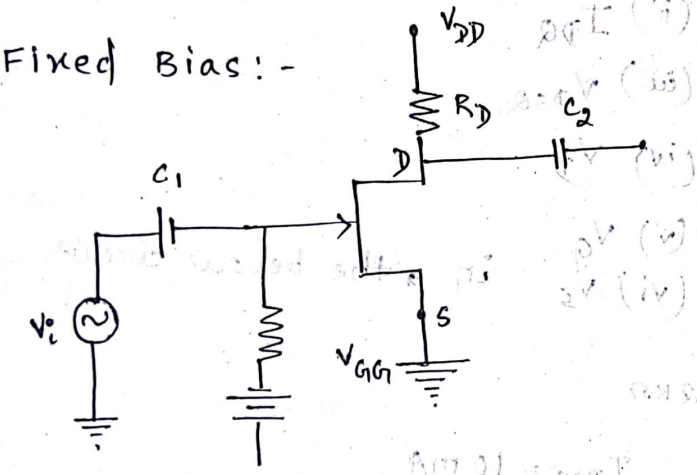


Biasing in JFET :-

→ It is needed for faithful amplification.
OR it is needed to get operating point.

→ In case of ;

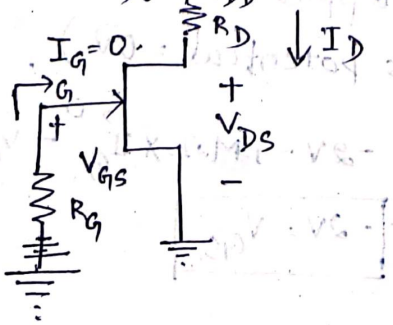
(i) Fixed Bias :-



For biasing, we need DC equivalent circuit :-

At DC, f = 0

$Z_C = \frac{1}{0} = \infty$, C = open circuit.



Applying KVL;

$$-V_{GG} - 0 \times R_G - V_{GS} = 0$$

$$\Rightarrow \boxed{V_{GS} = -V_{GG}}$$

$V_{DD} - I_D R_D - V_{DS} = 0$ → In outer KVL

$$\Rightarrow V_{DS} = V_{DD} - I_D R_D$$

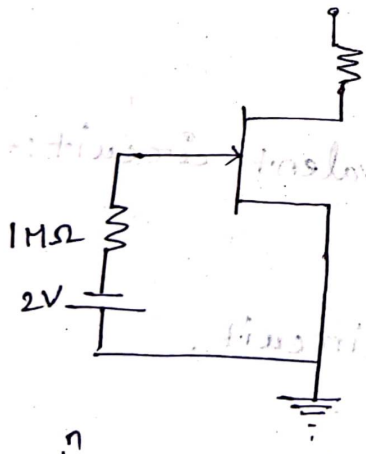
By shockeley's eqn;

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\Rightarrow \boxed{I_D = I_{DSS}\left[1 + \frac{V_{GG}}{V_P}\right]^2} \quad (\because V_{GS} = -V_{GG})$$

$$V_{DS} = V_{DD} - \left[1 + \frac{V_{GG}}{V_P}\right]^2 R_D I_{DSS}$$

Q:- Determine (i) V_{GSQ}
(ii) I_{DQ}
(iii) V_{DSQ}
(iv) V_D
(v) V_G
(vi) V_S in the below circuit.



$I_{DSS} = 10\,mA$

$|V_P| = 8V \Rightarrow \boxed{V_P = -8V}$

→ solve this by graphical approach.

Sol:- $V_S = 0V$. (Ground's potential = 0V).

Applying KVL; $-2V - 1M\Omega \times I_G - V_{GS} = 0$

($\because I_G = 0V$)

$$\Rightarrow \boxed{-2V = V_{GS}}$$

$V_{GS} = V_G - V_S$ ($V_S \to 0$)

$\Rightarrow -2V = V_G$

$\Rightarrow \boxed{V_G = -2V}$

$$I_D = I_{DSS}\left[1 - \frac{(-2)}{(-8)}\right]^2$$

$$= 10\left[1 - \frac{1}{4}\right]^2$$

$$= 10\left[\frac{3}{4}\right]^2$$

$$= 10\left(\frac{9}{16}\right)$$

$$= \frac{45}{8}\ mA.$$

$$= \frac{90}{16}$$

$$= 5.62\ mA$$

$\therefore I_D = 5.62$

~~5.62 mA~~

$16 - 2 \times 5.62 - V_{DS} = 0$

$\Rightarrow \boxed{V_{DS} \simeq 4.75\ V}$

$V_{DS} = V_D - V_S$ ($V_S \to 0$)

$\Rightarrow \boxed{4.75 \simeq V_D}$

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Graphical Approach :-

Applying KVL, in an input loop ;

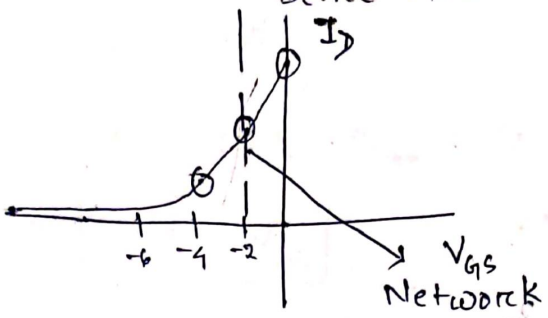
$-V_{GG} - 0 \times R_G - V_{GS} = 0$

$\Rightarrow -2 - 0 - V_{GS} = 0$

$\Rightarrow \boxed{V_{GS} = -2V}$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = 10\left(1 + \frac{V_{GS}}{8}\right)^2\ mA.$$

Device characteristics.



Network characteristics.

$V_{GS} = 0$, $I_D = I_{DSS} = 10\,mA$

$V_{GS} = -1$, $I_D = 0A$

$V_{GS} = -4$, $I_D = 2.5\,mA$

$V_{GS} = -2$, $I_D = 5.62\,mA$

From the graph $I_{DQ} =$

Applying KVL at output loop,

$$16 - 2K I_D - V_{DS} = 0$$

$$\Rightarrow 16 - 2K \times 5.62 = V_{DS}$$

$$\Rightarrow 4.76\,V = V_{DS}$$

$$V_D - \cancel{V_S}^{0} = V_{DS}$$

$$\Rightarrow V_D = V_{DS}$$

$$\Rightarrow V_D = 4.76V.$$

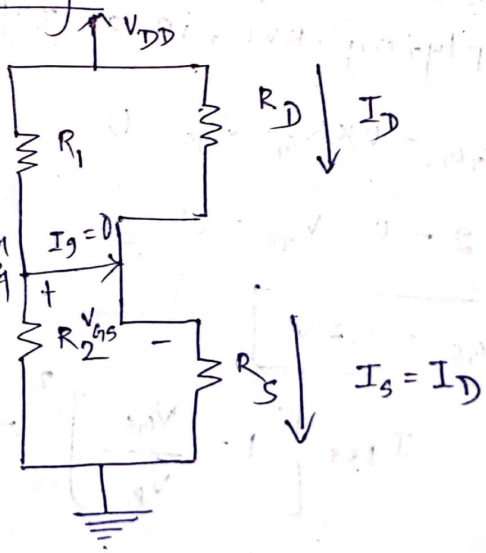
$$V_{GS} = -2V.$$

$$\Rightarrow V_G - \cancel{V_S}^{0} = -2V$$

$$\Rightarrow V_G = -2V.$$

Voltage divider biasing :-

circuit diagram;



In case of FET,

$I_D = I_S$ always.

$I_g = 0$.

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

Applying KVL in input loop :-

$$V_2 - V_{GS} - I_D R_S = 0$$

$$\Rightarrow \boxed{V_{GS} = \frac{V_{DD} R_2}{R_1 + R_2} = I_D R_S}$$

By shockley's eqn ;

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\Rightarrow \boxed{I_D = V_{DSS} \left[1 - \left(\frac{\frac{V_{DD} R_2}{R_1 + R_2} - I_D R_S}{V_P} \right) \right]^2}$$

Applying KVL at output ;

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\Rightarrow \boxed{V_{DS} = V_{DD} - I_D R_D - I_D R_S}$$

Q (V_{DS}, I_D)

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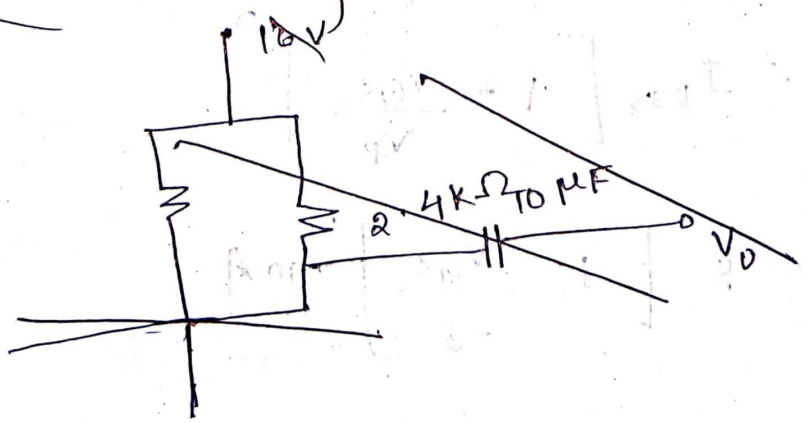
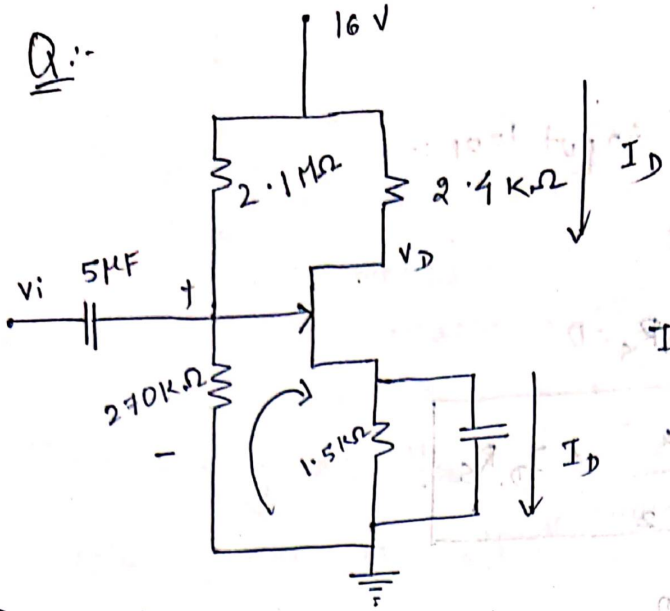
Determine the following from the figure below :-



28/10/2019

Q:-



$I_{DSS} = 8\ mA$

$V_P = -8\ V$

Determine the following :-

(i) I_{DQ}, V_{GSQ}

(ii) V_D

(iii) V_S

(iv) V_{DS}

(v) V_{DG}

Ans :- $V_G = \dfrac{16 \times 0.27\ M\Omega}{2.1\ M\Omega + 0.27\ M\Omega}$

$= \dfrac{16 \times 0.27}{2.37} = 1.82\ V$

$I_D = I_{DSS}\left[1 - \dfrac{V_{GS}}{V_P}\right]^2$

$= 8\left[1 - \dfrac{V_{GS}}{-8}\right]^2 mA$

$1.82 - V_{GS} - 1.5K I_D = 0$

$= 1.82 - 1500\ I_D$

$$I_D = 8\left[1 + \frac{1.82 - 1500 I_D}{8}\right]^2$$

$I_D = 2.4\,mA$ ~~7.8 mA~~ ~~-ve~~ } neglate these.

$V_S = 1.5\,K\Omega \times 2.4\,mA$

$= 3.6\,V.$

$V_{GS} = V_G - V_S = 1.82 - 3.6 = -1.78\,V.$

$16 - 2.4\,K\Omega \times 2.4\,mA - V_{DS} - 3.6 = 0$

$V_{DS} = 6.64\,V.$

$V_{DS} = V_D - V_S$

$\Rightarrow 6.64 = V_D - 3.6$

$\Rightarrow V_{DS} = 10.24\,V.$

$V_{DG} = V_D - V_G$

$= 10.24 - 1.82$

$= 8.42\,V.$

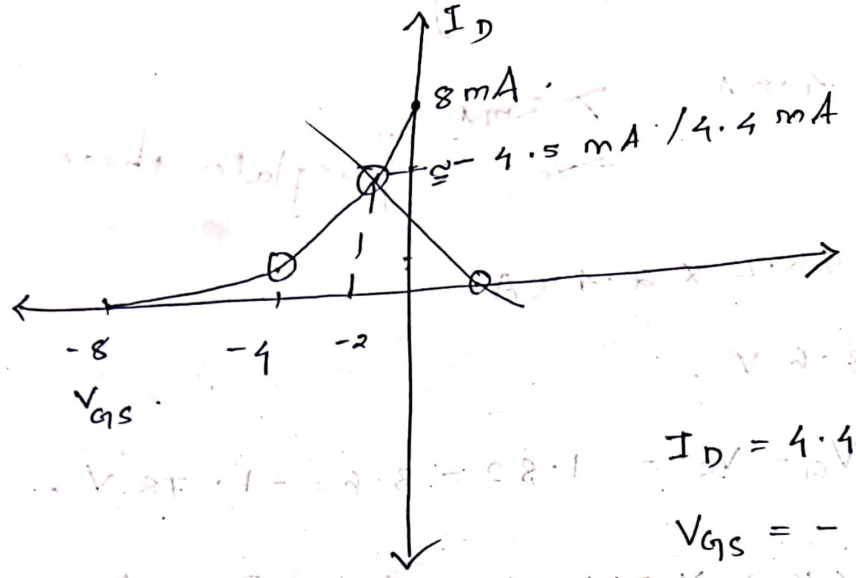
Graphical method :- $V_G = \frac{16 \times 0.27\,M\Omega}{2.1\,M\Omega + 0.27\,M\Omega}$

$= 1.82\,V.$

Applying KVL here,

$1.82 - V_G - 1.5\,K I_D = 0 \quad (I/P)$

$$I_D = 8\left[1 + \frac{V_{GS}}{8}\right]^2 mA.$$



$I_D = 4.4$ mA

$V_{GS} = -2$ V.

$V_{GS} = V_G - V_S$

$\Rightarrow V_S = V_G - V_{GS}$

$V_{GS} = 0$ V, $I_D = 8$ mA

$V_{GS} = -8$ V, $I_D = 0$

$V_{GS} = -4$ V, $I_D = 2$ mA

$V_{GS} = -2$ V. $I_D = 1.21$ m

MOSFET :-

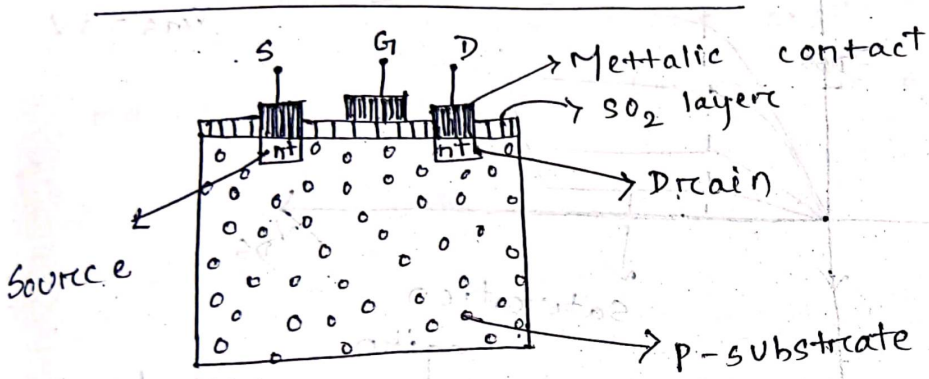
→ Metal oxide ~~free~~ ~~di~~ semiconductor field effect transistor.

→ It is said to be when isolation between gate and channel is done by SiO_2 layer.

→ MOSFET is classified into 2 types.

(i) DMOS (Depletion type MOSFET) present Whenever there is a channel bet^n source and drain, that MOSFET is DMOS.

Construction of DMOS :- 30/10/19



Construction :-

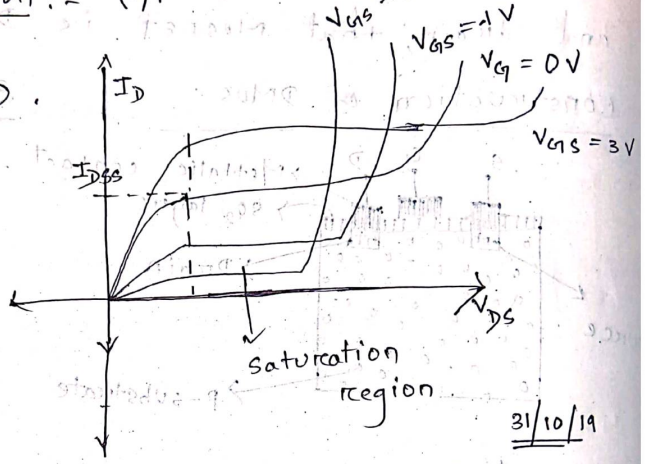
→ For ~~no~~ n-channel ~~dopr~~ D-typpe MOSFET consider a lightly doped p-type substrate in which 2 heavily doped n-type material are diffused on the two side of top layer which can treat as source and drain.

→ There is a channel present bet^n source and drain through which carrerr can move from source to drain.

→ On the top of drain & source metalic contacts are used to develop source & drain terminal.

→ To make isolation bet^n gate terminal & channel SiO_2 layer is used. And on the top of SiO_2 layer metalic contact is used to develop gate terminal.

Operation :- (o/p char. curve)



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→ Keeping $V_{GS} = 0V$ and $V_{GS} = 0V$, there will be no movement of carriers from source & drain through the channel. so, I_D current = 0.

By increasing V_{DS} +vely some electrons and source will get repelled and they enter in to channel and move to drain.

→ As a result, there will be movement of carriers source to drain through channel. As a result some I_D current

will be present.

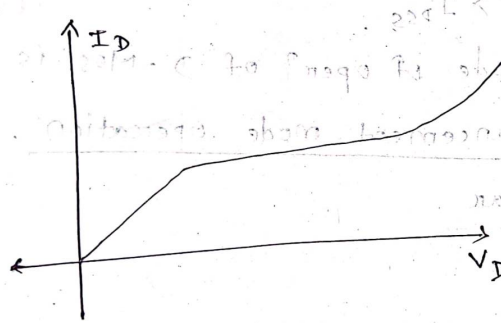
→ If you increase further, the value of V_{DS}, more no. of e^- will move from source to drain, as a result I_D will increase.

→ If we further increase the value of V_{DS}, I_D current will constant (not increase).

→ Because, channel is fulled or channel gets saturated.

→ If you further increase V_{DS} same constant current will flow from source to drain.

→ If we further increase V_{DS}, there will be breakdown & there will be sharp raise in current from drain to source.



→ V_{GS} = -ve, the e^- which are repelled by V_{DS} from source will be opposed by the app. of V_{DS}, so, I_D current gets reduced.

→ When V_{GS} = -ve pinch off will occur quickly. By increasing V_{GS} -vely I_D current get reduced and it will reached a $I_D = 0$.

→ the value of V_{GS}, at which I_D current = 0,

that value of V_{GS} is known as pinch off voltage.

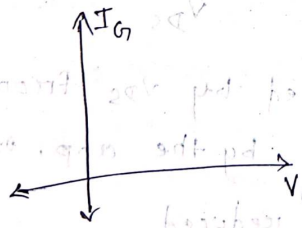
→ But taking V_{GS} +ve the e⁻ which are repelled by V_{DS} from source will be supported by applying V_{DS} supportively. so, I_D current gets increase.

→ If you further increase the value of V_{GS} +vely, I_D current gets increased, by further increasing V_{DS} +vely, I_D current greater than I_{DSS}.

$$I_D > I_{DSS}.$$

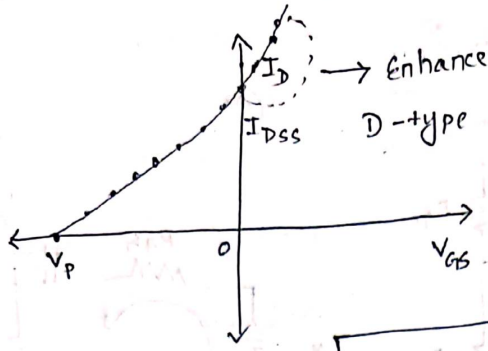
This mode of oper^n of D-Mos is known as enhancement mode operation.

I/P char



Transfer characteristics :-

It is the characteristics curve bet^n o/p current and i/p current.



→ Enhancement mode in D-type MOSFET.

Transconductance :-

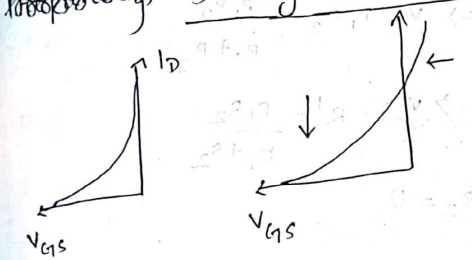
$$g_m = \frac{d I_D}{d V_{GS}}$$

$$= -\frac{2 I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

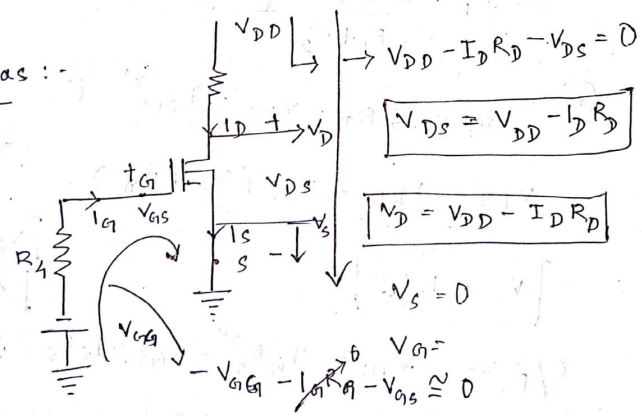
04/11/2019

Biasing of DMOS :-



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

① Fixed Bias :-



$V_{DD} - I_D R_D - V_{DS} = 0$

$\boxed{V_{DS} = V_{DD} - I_D R_D}$

$\boxed{V_D = V_{DD} - I_D R_D}$

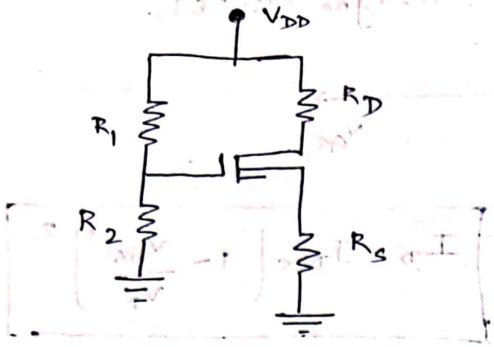
$V_S = 0$

$V_G =$

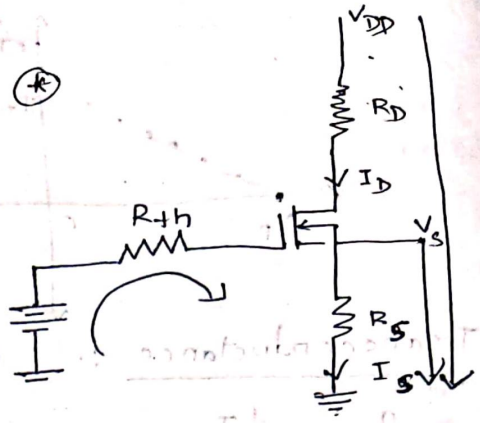
$-V_{GG} - I_G R_G - V_{GS} \cong 0$

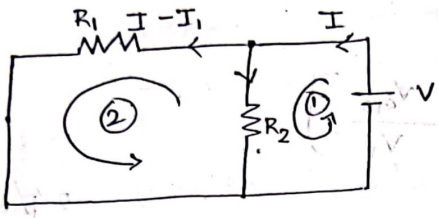
$\boxed{V_{GS} = -V_{GG}}$

② Voltage Divider :-



(*)





① $\rightarrow V - I_1 R_2 = 0 \Rightarrow V = I_1 R_2 = \dfrac{R_1 R_2}{R_1 + R_2}$

$\Rightarrow \dfrac{V}{I} = R' = \dfrac{R_1 R_2}{R_1 + R_2}$

② $-(I - I_1)R_1 + I_1 R_2 = 0$

$\Rightarrow I_1 (R_1 + R_2) = I R_1$

$\Rightarrow I_1 = \dfrac{R_1}{R_1 + R_2} I$

(*) $V_{DD} - I_D R_D - V_{DS} - \cancel{I_{DRS}}^{0} = 0$

$V_{DS} = V_{DD} - I_D (R_S + R_D)$

$\therefore V_{GS} = V_G - V_S$

$= V_{TH} - I_S R_S$

$\boxed{V_S = I_S R_S}$

$\boxed{V_{GG} = V_{GS} + V_S}$

$\boxed{V_{GG} = V_{TH}}$

i/p $\rightarrow V_{TH} - \cancel{I_G R_G}^{0} - V_{GS} - I_S R_S = 0$

$\Rightarrow \boxed{V_{GS} = V_{TH} - I_S R_S}$

To solve the biasing circuit 2 different approches can be adopted.

(1) Mathematical approch

(2) Graphical approch

Q:- For a voltage divided circuit,

$R_1 = 2.1\ M\Omega$ $R_2 = 270\ K\Omega$

$R_D = 2.4\ K\Omega$, $R_S = 1.5\ K\Omega$

$I_{DSS} = 8\ mA$, $V_P = -4\ V$.

Power supply = 16 V. Find out all the parameters using graphical & mathematical approch.

Soln:- Mathematical Approch:-

$$R_{TH} = R_1 \,||\, R_2 = 2.1\ M\Omega \,||\, 270\ K\Omega$$

$$= \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{2100 \times 270}{2100 + 270}$$

$$= \frac{567000}{2370} = 239.24.$$

1) $$V_{TH} = \frac{16 \times 270 \times 10^3}{2370 \times 10^3} = 1.82\ V$$

2) $$V_{GS} = V_{TH} - I_S R_S = 1.82 - I_S \times 1.5 \times 10^3$$

$$V_{GS} = 1.82 - 1.5 \times 10^3 I_D$$

3) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8 \times 10^{-3}\left(1 + \frac{1.32 - 1.5 \times 10^3 I_D}{4}\right)^2$$

$$\Rightarrow I_D = \frac{8}{18_2} \times 10^{-3} \left(5.82 - 1.5 \times 10^3 I_D \right)^2$$

$$\Rightarrow 2 I_D = \left[(5.82)^2 + (1.5 \times 10^3 I_D)^2 - 2 \times 5.82 \times 1.5 \times 10^3 I_D \right] \times 10^{-3}$$

$$\Rightarrow 2 I_D = \left[33.85 + 2.25 \times 10^3 I_D^2 - 17.46 I_D \right]$$

$$\Rightarrow 2250 I_D^2 - 19.46 I_D + 33.85 \times 10^{-3} = 0$$

$$\Rightarrow I_D = \frac{19.46 \pm \sqrt{(-19.46)^2 - 4 \times 2250 \times 33.85 \times 10^{-3}}}{2 \cdot 2250}$$

$$= \frac{19.46 \pm \sqrt{378.69 - 304.65}}{4500}$$

$$= \frac{19.46 \pm \sqrt{74.04}}{4500}$$

$$= \frac{19.46 \pm 8.60}{4500}$$

$$= \frac{19.46 + 8.60}{4500} = 6.23 \times 10^{-3} = 6.2 \text{ mA}$$

and $\frac{19.46 - 8.60}{4500} = 2.41 \times 10^{-3}$

$= 2.4 \text{ mA}$.

steps for find I_D :-

→ If the obtained I_D values has one -ve & +ve value of I_D, then select the +ve value, of I_D as I_{DQ}.

→ If both the values of I_D are +ve, put each the values of I_D in the V_{GS} eqn & find out the value of V_{GS}, which lies betn 0 and V_p. That becomes V_{GSQ} and the corresponding I_D value becomes I_{DQ}.

→ If both the V_{GS} value lies betn 0 & V_p then solve by graphical approach to find out I_{DQ} & V_{GSQ}.

$$-V_{GS} = 1.82 - 1.5 \times 10^{3} \times 6.2 \times 10^{-3}$$

$$= 1.82 - 9.3 = -7.48$$

$$V_{GS} = 1.82 - 1.5 \times 10^{3} \times 2.41 \times 10^{-3}$$

$$= 1.82 - 3.61$$

$$V_{GS} = -1.79 \text{ V}$$

$$I_D = 2.4 \text{ mA}.$$

Enhancement type MOSFET (E-MOS) 06/11/19

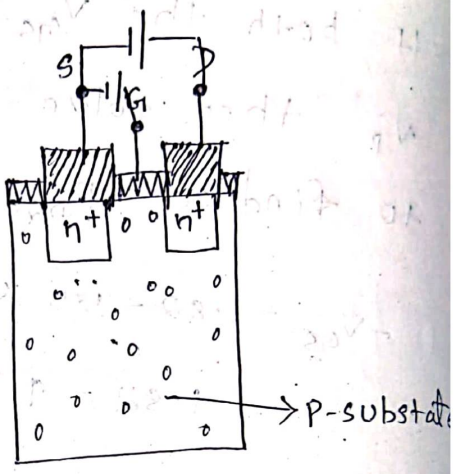
n-channel E-MOS | p-channel E-MOS

→ In this type MOSFET, initially there is no chance bet^n source & drain, we have to enhance the channel bet^n source and drain by application of V_{DS}.

Construction :-

N-channel E-MOS :-

→ For this consider a P-substrate and two heavily dopped n-type material are defused on the 2 sides of on the top of P-substrate.



→ Which may lead to from source & drain and on the top of heavily dopped n-type material. metalic contacts are used to form source & drain terminal.

→ to make Isolation bet^n channel & gate SiO_2 layer is present above the channel region, and on the top of SiO_2 layer, metalic contact is used to form the gate terminal.

Operation :-

→ Keeping $V_{GS} = 0$, and by increasing V_{DS} there will be no movement of carriers from source to drain, bcoz there is no channel. As a result I_D current = 0.

→ To establish the channel, we have to increase V_{GS} +vely, when $V_{GS} \gg V_{TH}$ then channel will be establish.

→ By appln of V_{GS} = +ve, the holes in the channel region will be repelled by gate terminal & minority character of P-substrate will be attracted & this e^- will be deposited underneath of gate terminal.

→ When $V_{GS} \gg V_{TH}$, channel region will be free of holes & only free e^- will flows. and hence channel is established.

→ When $V_{GS} < V_{TH}$, by application of any V_{DS} I_D current is 0.

Threshold voltage (V_{TH}) :-

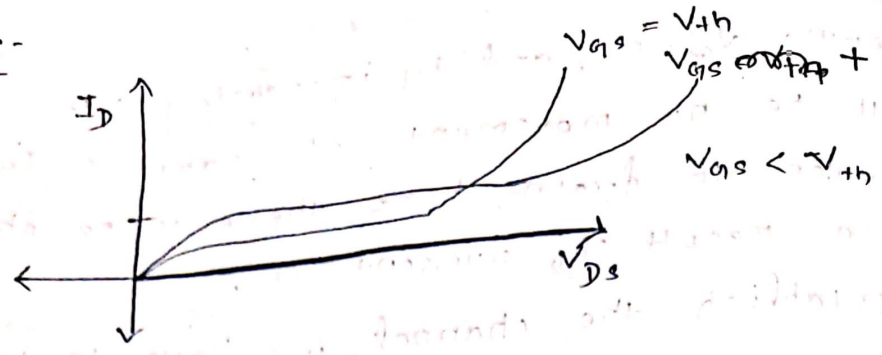
The value of V_{GS} at which channel is established, that value of V_{GS} is known as Threshold voltage.

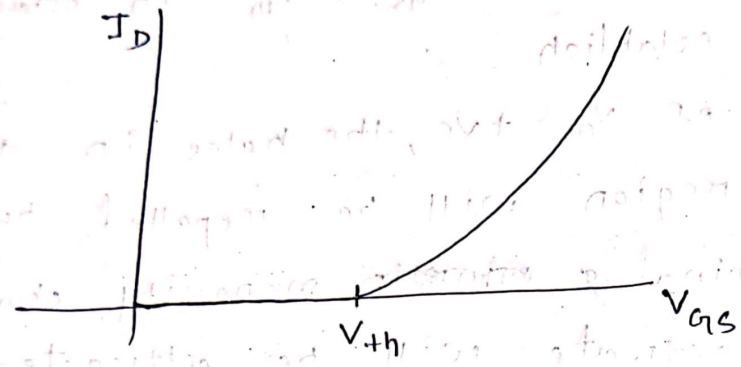
Note :-

V_{TH} is +ve for N-type E-MOS.

V_{TH} is -ve for P-channel E-MOS.

O/P :-





→ Current eqⁿ in the saturcation region is not satisfying by the circle's eqⁿ.

So, current in the saturcation region is given by, $\boxed{I_D = K(V_{GS} - V_{th})^2}$

Value of K depends on the aspect ratio and dielectric bet^n gate & channel & so on.

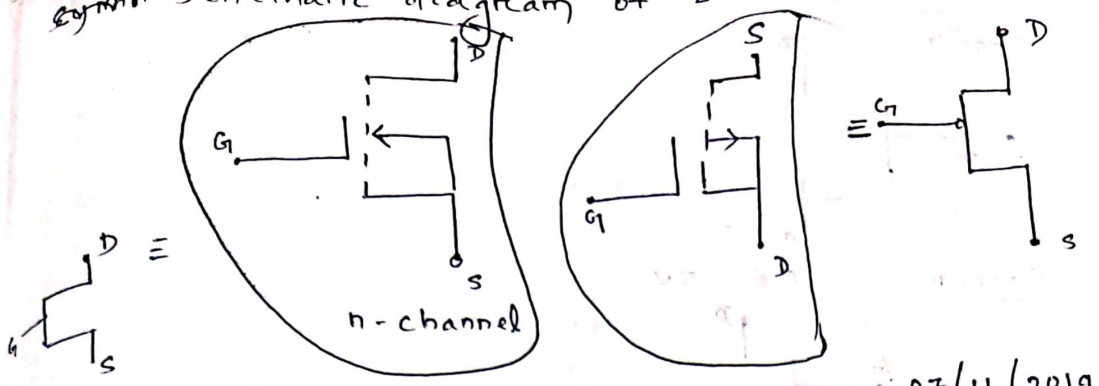
Aspect ratio : $\frac{W}{L}$ → width of channel
→ Length of channel.

Transconductance :-

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$\Rightarrow g_m = 2K(V_{GS} - V_{th})$$

Symbol schematic diagram of E-MOS.



07/11/2019

CMOS (Complementary Mos)

logic

+ve logic — -ve logic

logic level :-

→ When bit 0 or bit 1 is assign to a voltage level, process is known as logic level.

logic level can be 2 types.

(1) +ve logic level -

In this higher voltage value is assigned to bit 1 and lower voltage level is assigned to bit 0.

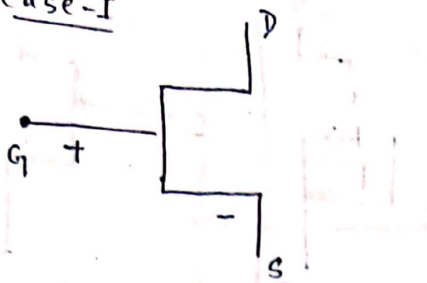
(2) -ve logic level.

similarly in this, lower is assigned to bit 1 and higher is assigned to 0.

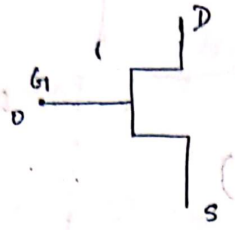
bit	+ve logic	-ve logic
1 → 5 V	-5 V → bit 0	1 → -5 V, 0 → +5 V
1 → 5 V	0 V → 0	1 → 0 V, 0 → 5 V

N-MOS :-

Case-I



Case-II



0 ≡ -5V

1 ≡ 5V

→ To transmit bit 0 from source to drain by n-Mos is possible. But, n-Mos has inability to transmit bit 1 from source to drain.

→ Similarly by p-Mos we can send bit 1 from source to drain and p-Mos has inability to send bit 0 from source to drain.

→ In above 2 cases inability is bcoz of no channel, betⁿ source & drain.

Bcoz of this inability p-Mos is always connected to +ve voltage and N-Mos is always connected to ground.

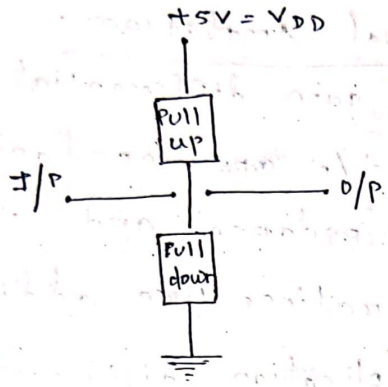
This stᴿ is known as c-Mos.

→ c-Mos consists up two network.

1. Pull up
2. Pull down

In which, pull up is always connected to voltage and pull down is always connected to ground.

→ Pull up network consists up only P-MOS.
Pull down " " " " N-MOS.

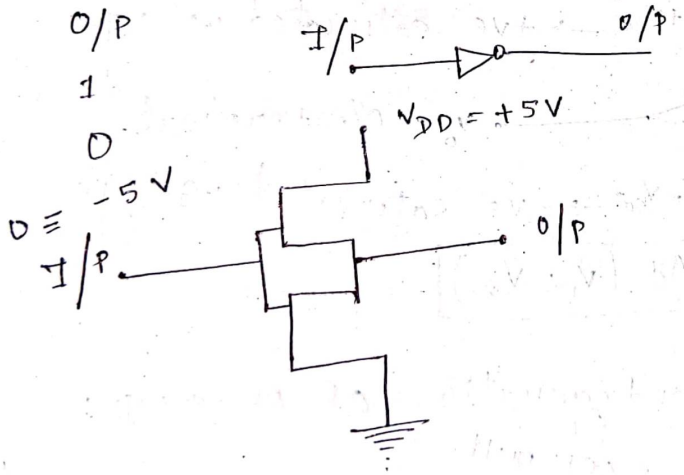


Application :-

C-MOS has inverted (NOT Gate)

Truth table

I/P	O/P
0	1
1	0

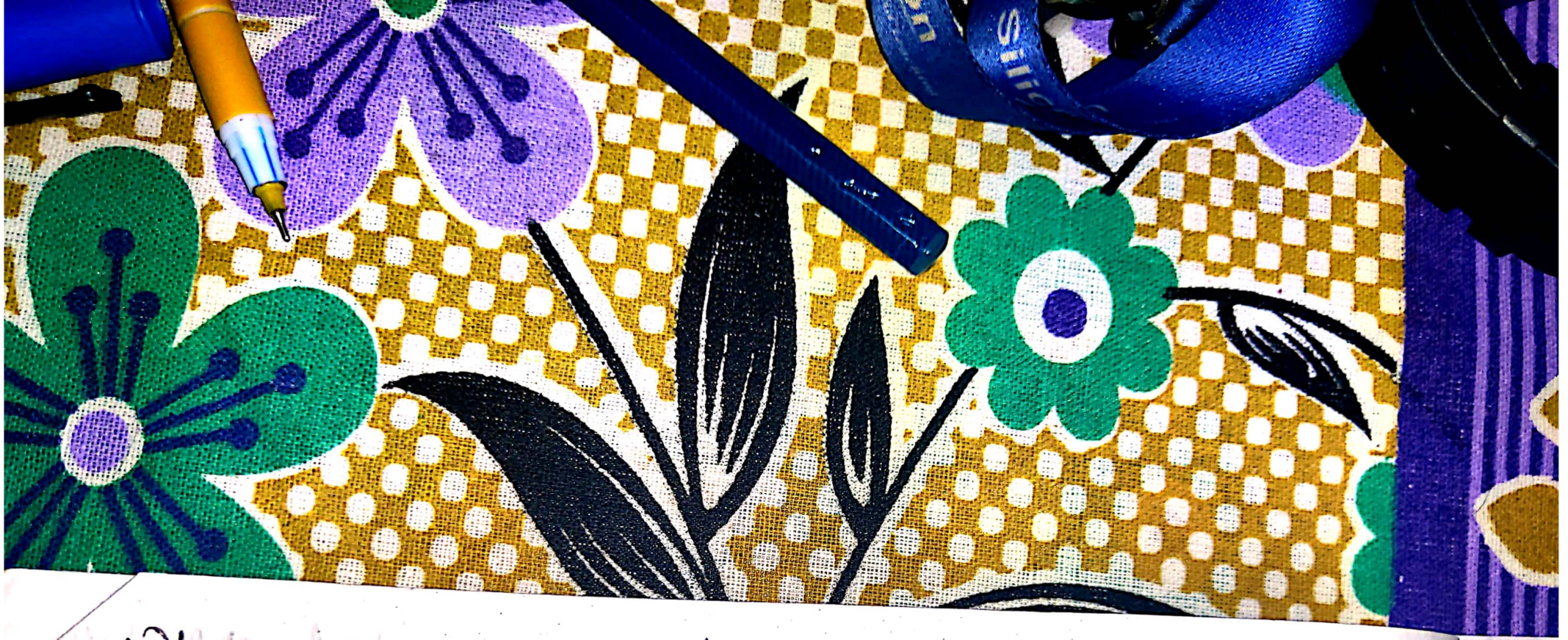


When logic 0 as input :-

logic = 0 means 0V.

for n-mos, $V_{GS} = 0V$ ⇒ No channel i.e; open circuit bet^n S → D.

for P-MOS, V_{GS} = -ve ⇒ Channel established short circuit bet^n S → D.



When logic = 1 at I/p :-

For n-MOS, $V_{GS} = 5V \Rightarrow$ channel i.e; short circuit bet^n S → D.

For p-MOS, $V_{GS} = +ve \Rightarrow$ channel established short circuit S → D

UNIT-IV